Accelerate FPGA Designer Productivity with the ISE Design Suite

Agenda

- **Challenges of modern FPGA design**
- **Shortening the FGPA design flow**
  - Design creation
  - Implementation
  - Analysis, verification, debugging
- **Conclusion**

The Need to Conquer the Productivity Challenge

$$\text{Design Labor Cost} = \frac{\text{(labor unit cost) x (design complexity)}}{\text{designer productivity}}$$

"To avoid exponentially increasing design cost, overall productivity of designed function on a chip must scale at > 2X per technology generation."

Source: International Technology Roadmap for Semiconductors, 2008

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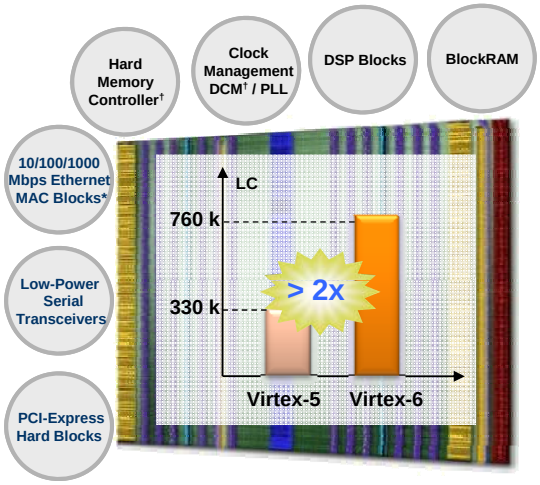
Today's FPGA Design Challenges

- **FPGA complexity doubles every new generation**
  - More Logic
  - Embedded IP Cores
- **Pressure to improve productivity and reduce design cycle**
- **Various design criteria must be met simultaneously:**
  - Timing, power, cost, ...



Xilinx Provides Tools and IP Cores Accelerating Your Productivity by Meeting Design Goals Faster

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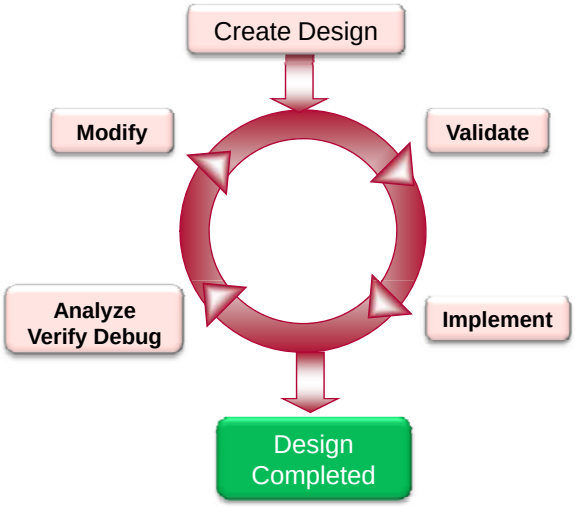
Shortening the FPGA Design Flow



Design Goals

- Timing Closure
- Power Budget
- Bug Free
- • •

Increase Productivity by

- **Accelerating Each Design Step**
- **Reducing Number of Iterations**

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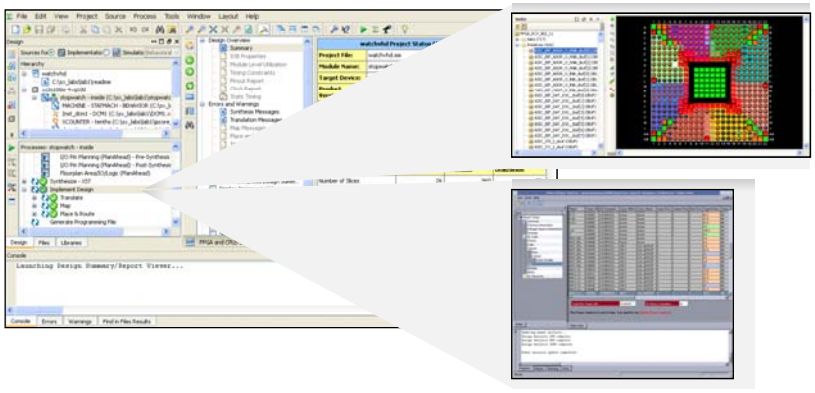
Project Navigator and the ISE Design Environment

Easy & Fast Way to Control
Design Flow from a Unique Design Cockpit

XILINX® ISE® DESIGN SUITE



- **ISE allows to plug and use 3rd party tools**
  - Synthesis and Simulation from leading EDA providers

Optimizing Design Entry

Helping You to
Focus on Your Product Differentiation

- **Key Features:**
  - Supports multiple personas: Logic, DSP, Embedded, ...
  - Reuse methodology: vast IP support, create your own libraries
  - Early Pin and FloorPlanning
  - Easy Design Constraining

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XST – Xilinx Synthesis Technology

RTL: **Higher Productivity**
Easy Retargetable Designs

- **Strong compliance to IEEE HDL Standards results in**
  - Higher productivity via more freedom in coding styles
  - IEEE HDL Standards Compliant
    - VHDL: IEEE 1076-1993
    - Verilog: IEEE 1364-2001
- **Same Functionality with reduced amount of RTL code**
  - Higher Level of abstraction supported by Synthesis (XST)
  - Compact description of complex functions: RAM, DSP, ...
  - Retargetable code to multiple architectures

Accelerating Design Entry with IP Cores

IP Cores: **Reduce Development Time**
Accelerate Time-to-Market

- **FPGA Industry's Most Extensive IP Portfolio**
- **Wide range of IP from Xilinx and Alliance Partners:**
  - Connectivity, DSP, Embedded Processing
  - Application segments: Communications, Consumer, Automotive, Medical, Industrial, Aerospace & Defense etc.
- **Focus your engineering on your product differentiation**
- **Optimized for Xilinx FPGA**
  - Proven quality & cost effective

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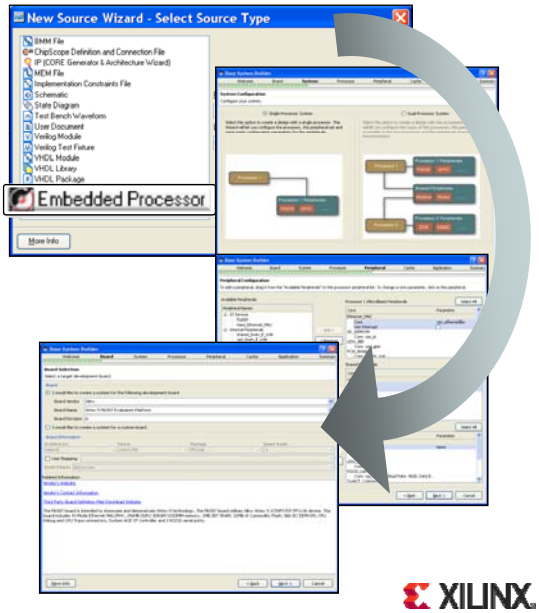
Design Entry for Embedded Design

Platform Studio: **Fast Manner to Create Embedded Processor Designs**

- **Key Features**
  - Fully integrated in ISE flow
  - Automatic creation of single or dual processor systems
  - Easily connect peripherals to all processors in system
  - Automatically selects the board matching the target device



Design Entry for DSP Design

System Generator: **High-Performance DSP Systems in a Fraction of Traditional RTL Development times**

- **Key Features**
  - Develop highly parallel systems
  - System modeling and automatic code generation from Simulink® and MATLAB®
  - Hardware Co-Simulation

Accelerate Simulation up to **1000x**

  - Hardware / software co-design of embedded systems
    - Build and debug DSP co-processors for the Xilinx MicroBlaze™ processor core.

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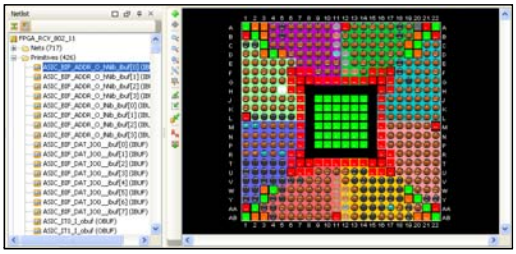
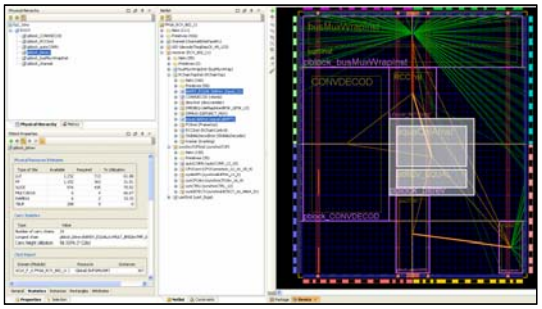
Pin Planning and Hierarchical Floorplanning

- **Early Pin Planning**
  - Easy Drag & Drop IO Assignment
  - Semi-automatic placement modes for interfaces in few mouse clicks
  - DRC check on the fly



- **Hierarchical Floorplanning**
  - Export & reuse IP modules
  - Shortens design implementation by guiding place and route
  - Robust block creation capabilities



Optimizing Implementation

Our Focus: **Two Main Directions to Shorten Implementation Flow**

- **Faster runtime of each implementation step**
  - Synthesis, MAP, PAR, ...

- **Meet design goals faster by**
  - Increasing optimizations efficiency
  - Using innovative methods:
    - Incremental flow
    - Tasks distribution across a network

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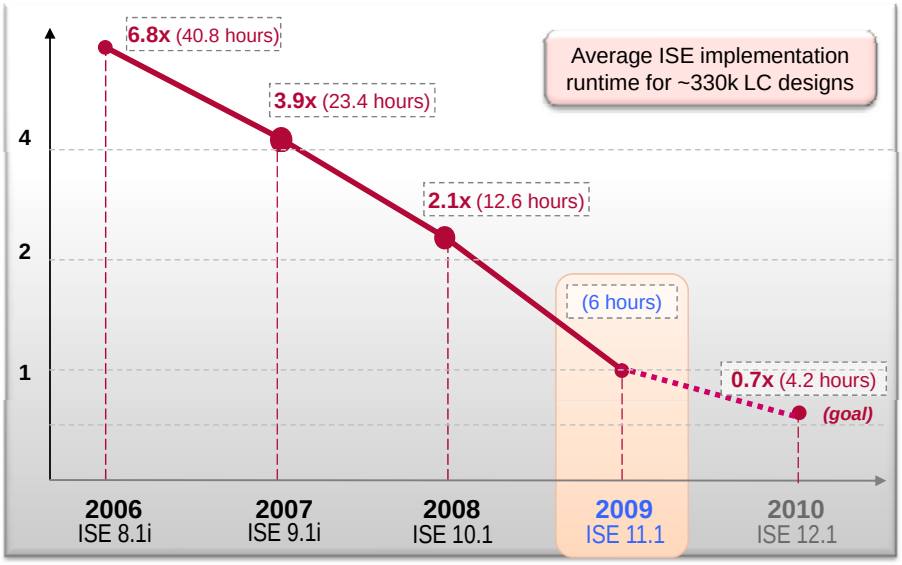
Improving Implementation Run Times

Faster Consecutive Implementations Using Faster Synthesis, Map, Place & Route



Runtime Normalized to ISE 11.1

- **Achieved via**
  - New faster algorithms
  - Multithreading

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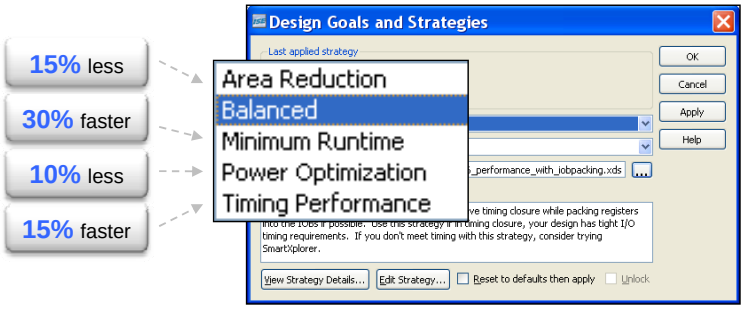
Goal-Based Implementation

Meet Design Requirements Easier via Dedicate Optimization Methods

- **Powerful optimizations methods targeting key goals**
  - Entire flow easy setup via predefined design strategies
  - Automates:
    - Retiming / Pipelining
    - Power Optimization
    - Clock Gating
    - LUT Combining
    - Area optimization
    - ...



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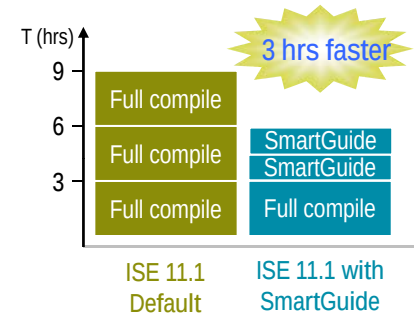
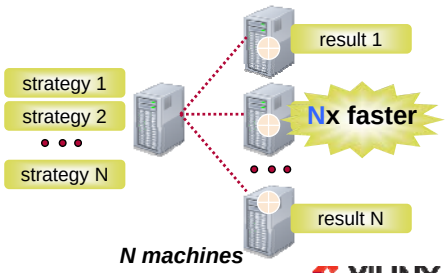
Innovation in Implementation

SmartGuide: **Dramatic Total Development Time Reduction**
SmartXplorer:

- **SmartGuide: Incremental Implementation**
  - Dedicated to small design changes
  - Limits place & route to changed portion of the design
- **SmartXplorer: Fast means to timing closure**
  - Best timing closure predefined strategies
  - Parallel strategies execution across a network
    - LSF/SGE support (acronym)





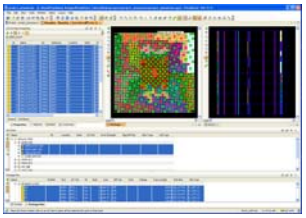
Optimizing Analysis, Verification, and Debugging

Powerful Analysis, Verification, Debugging
Keys for Fast Design Closure

- **Automatic DRCs capabilities across the entire flow**

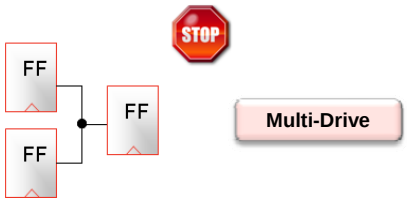
Example 1

– Powerful DRC checks during pin-planning
Including WASSO analysis



Example 2

– Automatic detection of bad design practices in XST



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Customizing Synthesis Checks

Avoid Design Errors by Defining Custom Design Rule Checks

- **Benefits**
  - Errors detection at early design stages
  - Integrate custom checks in reusable blocks
  - Share the rules with your team
- **Implemented via**
  - assert (VHDL)
  - $finish/$display (Verilog)
- **Supported by XST**

VHDL

```
...
 assert SRL_WIDTH <= 17
     report "Shift Register Size must be <= 17 bits"
     severity FAILURE;
...
 inst2: SINGLE_SRL generic map (SRL_WIDTH => 18) ...;
```

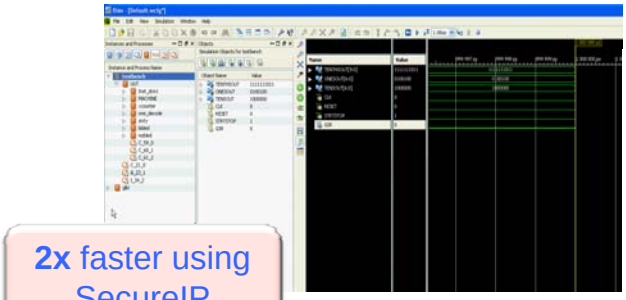
LOG

```
ERROR:Xst:1749 - test.vhd line 15:
      FAILURE: Shift Register Size must be <= 17 bits
```

Integrated Simulation with the ISE Simulator (ISim)

ISim: **Powerful, Fast & EOU Verification Tool Available in ALL Software Editions**

- **Simulate your design at each major design step**
  - RTL / Timing post PAR
- **Key Features**
  - Mixed VHDL/Verilog support
    - VHDL: IEEE 1076-1993
    - Verilog: IEEE 1364-2001
  - Supports all HardIPs (PowerPC, MGT, PCI, etc.)
  - Strong debug capabilities
  - Supports power analysis and optimization via SAIF

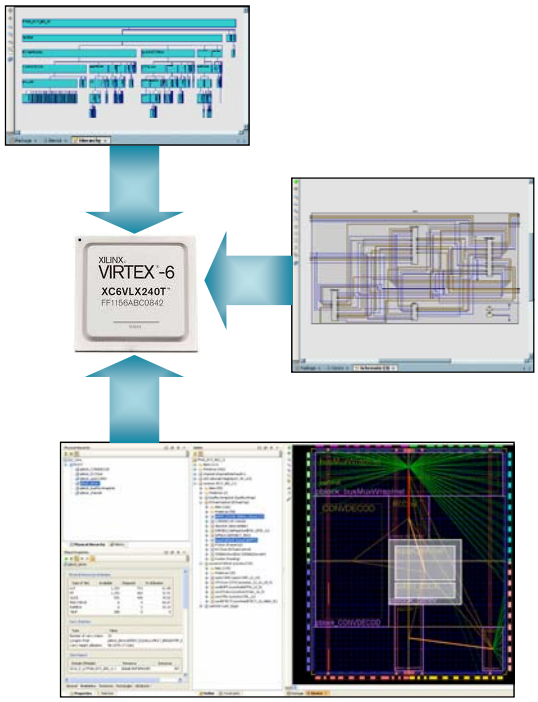


2x faster using SecureIP

PlanAhead for Optimal Design Analysis

Faster Design Closure 30% Better Performance

- **Quickly identify design bottlenecks**
  - Visibility into design from different angles (Schematic, Device, Netlist, Timing, ...)
  - One-click navigation between different views
  - All views cross-probe
- **Faster Timing closure**
  - Quickly identify, select, constrain critical logic
  - Hierarchical Floor-Planning
- **Reuse Successful Results**
  - Fix logic placement for future runs



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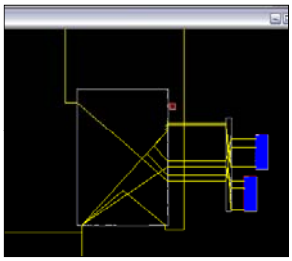
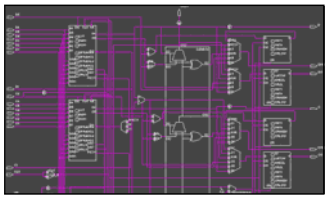
FPGA Editor for Editing and Exploration

FPGA Editor: Accurate Design Exploration
Rapid Editing

- **Most accurate design exploration**
  - All FPGA elements are visible (slice, IOs, ...)
  - With exact placement and
  - Precise routing topology



- **Ultimate user control over design implementation**
  - Rapid post-route design editing (logic, placement, routing)
  - No re-implementation required

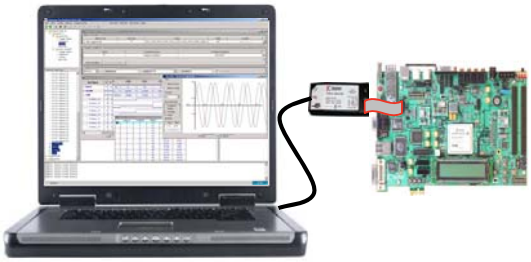


- **Great for architecture evaluation – no design required**

ChipScope Pro for On-Chip Debug

ChipScope® Pro: **On-Chip Debugging 2x Faster**

- **Monitor and Debugging**
  - Actual system and actual speeds
- **Supports multiple personas:**
  - Logic, DSP, embedded, ...
- **Key Features**
  - Monitor any internal signal
  - Easy one-click debug signals selection
  - No need to re-implement the design
  - Integration with Agilent logic analyzers
  - Monitor thermal & voltage data via System Monitor



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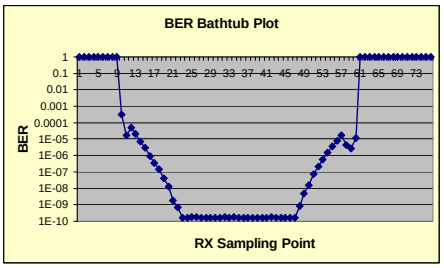
ChipScope Pro Serial I/O Toolkit

- **Enables Integrated Bit-Error Ratio Testing (IBERT)**
- **Fast and easy debug of multi-gigabit transceivers**
- **Perform on-chip bit-error ratio (BER) tests**
  - Sweep-based margin analysis
- **Benefits:**
  - Alternative to costly external BERT measurement equipment



ChipScope Pro and Serial IO Toolkit Available in ALL Software Editions

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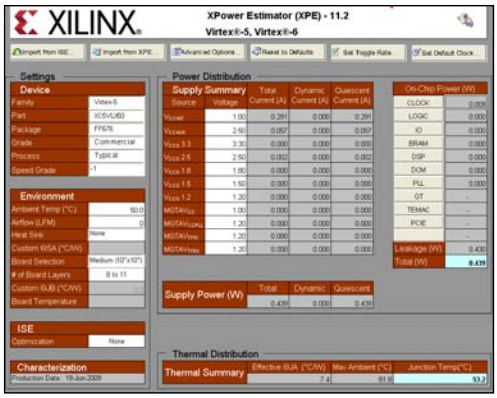
ISE Design Suite Enables a Complete Power Strategy

- **Power – one of the most critical FPGA design aspects today**
- **Correct power and cooling - foundation for a reliable system**

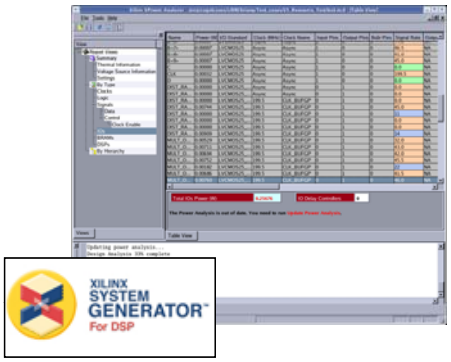
Plan, Monitor and Reduce Design Power Using Advanced Power Tools

- **Planning: XPower Estimator (XPE)**
  - Determines power requirements prior to design creation
  - Enables to evaluate different hardware implementation power tradeoffs via "what-if" analysis



Power Reduction and Analysis

- **Monitoring: XPower Analyzer (XPA)**
  - Precise and detailed power data for implemented design
  - Vector-based (SAIF) and vector-less analysis
  - Helps focus on critical areas
  - Integration with System Generator for DSP
    - Evaluation of DSP algorithmic and hardware solutions



- **Reduction:**
  - Use predefined power optimization strategies
  - Various design tips and hints available on WEB:
    - ***Power Consumption at 40 and 45 nm***
    - ***Virtex-5 FPGA System Power Design Considerations***
    - ...

10% dynamic power less

Summary

ISE Design Suite

- Unique and powerful design tools
- Allowing to accelerate time-to-market and
- Meet design goals

Start Your Design Today!
Additional Resources

1. Learn more at www.xilinx.com/ise
2. Additional videos are available at www.xilinx.com/design
3. Download a 30-day evaluation at www.xilinx.com/ise_eval
4. Begin your Virtex-6 or Spartan-6 design today with a Xilinx Targeted Design Platform at www.xilinx.com/kits
5. Visit www.xilinx.com/education to get the most out of ISE Design Suite with targeted, high-quality training

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