Aerospace Products Radiation Policy

Overview

Higher performance, speed, power consumption and cost are key words designers have to keep in mind in order to succeed in a fast changing and competitive world wide market.

However, before they finally accomplish their dream, their desires often turn into nightmares. This is mostly because new generation components use very aggressive technologies, primarily developed for commodity applications. In some cases, additional needs (e.g., Temperature, Reliability, Longevity, etc.) cannot be completely satisfied. This is obvious for all radiation harsh environments where Mean Time Between Failure (MTBF) relative to radiation induced defects is the driving factor for component selection policy.

In fact, high density commercial technologies are not characterized for their tolerance to radiation. Although some test results exist, commercial process changes, driven by performance and competitiveness can cause drastic variation in the radiation hardness from lot to lot, or even from wafer to wafer. We must not envisage procurement from distributors with stock parts with various date codes and mask and technology revisions.

From the beginning, Atmel has recognized that the continuation of this activity is linked to the capability to offer the designer access to state-of-the-art technology and products, which is synonymous with reactivity and duality. This is illustrated by the recent withdrawals of major component manufacturers from the Military and Space markets. On top of that, the radiation levels required by the applications were studied with remarkable outcomes: even though most of the radiation hardened applications (space, military, etc.) do not require more than 100 Krad (Si), the increased satellite longevity of LEO's share pushes the needs above 100 Krads.

Dual Use Concept

Because of general budget restrictions, dedicated component manufacturers who previously developed specific technologies and products for military applications are no longer supported by National agencies. However, investments necessary to improve technology performance, to shrink lithography, etc. are so high that few companies are prepared to bear the costs. The policy that Atmel decided to pursue is based on the translation of technology and products originally developed for large volume commercial markets (consumer, automotive or industrial) with basically no design and layout changes.

The radiation levels are those the applications require, the performance is what competitive markets require.

In space, emerging new large volume markets (e.g., New equipment for High Energy Physics) have changed the approach. New technologies, originally developed to use specific recipes and tools, can benefit from the dual use approach, in the sense that they can be transferred later in the development phase to a commercial manufacturing line using the techniques and equipment largely used for any other commercial business.

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Rev. 4170E–AERO–06/03

Using Atmel Radiation Hardened CMOS VLSI in Harsh Environments

In the past it was believed that almost all military and space applications could find solutions in dedicated databooks from sponsored component manufacturers. This is less and less true. On one side, the sponsors are threatened by budget restrictions; on the other hand, performance needs associated with competitiveness in a new open commercial space market, have reduced the offer. Despite their attempts to use commercial off the shelves components and technologies, designers are still forced to deal with the natural environment and its extreme working conditions. Beside these usual application fields, some emerging requirements arise. They come mostly from civilian nuclear research areas where it was common to use discrete or even passive components. In fact, MRAD is the basic unit these new applications have to tolerate.

Apart from the standard radiation induced damage known and treated in numerous studies for more than 30 years, this section will try to discuss new items such as Dose rate effects, voltage influence, efficiency of SEU tolerant cells and general technology shrink effects on SEU sensitivity. Then, future technology trends and their effects on radiation hardness will be presented.

The Environments

Space Systems

Mainly arising from the Earth's magnetosphere field, the Earth's particle charged belts (Van Allen Belts):

- Proton trapped belt, from 400 to 900 km, consists of electrons and protons.
- Electron trapped belt, extending up to 56,000 km, is almost entirely composed of electrons.

Irregular intense bursts associated with solar flares consisting of high energy protons and heavy ions, increasing the Van Allen Belt by a factor of 10^3.

Galactic cosmic rays composed of heavy ions from Hydrogen to Nickel in varied abundance: protons (85%), alpha particles (13%), heavy nuclei (2%).

Electrons and protons interact with material they encounter (any shielding material from the spacecraft body, packaging of the component, etc.) and electromagnetic rays (X and γ rays) are produced by the conversion of the primary radiation (Bremsstrahlung). These particles ionize the target material at very low dose rate (typically, less than 1 rad/hour), so only long term accumulated effects are of importance. Protons can interact directly with material and create heavy particles by nuclear reaction. No practical shielding is effective against heavy ions.

Component radiation hardness depends on the orbit and the time frame of the mission. Effect from the particles can be modeled, taking into account spacecraft structure and environment models to predict the radiation environment of a dedicated chip.

Nuclear Weapons

The nuclear blast environment is a function of the weapon yield, the distance from the blast, etc. Basically, a burst of γ followed by a second burst of neutrons depicts quite simply the nuclear detonation environment. ElectroMagnetic Pulse (EMP) is also of importance for electronics and all electrical conducting material.

Radiation Effects on CMOS VLSI

Surface Effects

X-rays, γ rays and electrons create ionization in SiO_2 by electron-hole generation. Due to combination effects and mobility difference between e-h, a positive layer is created in the Si-SiO_2 interface region in gate and field oxides. This effect induces shifts in basic device characteristics, i.e., threshold voltage and mobility.

The predominance of each contributor is technology and dose rate related and may vary from one vendor to another; however, one can consider that basically, ΔVt is negative for a N transistor and positive for a P transistor. At higher dose, the interface state generation becomes preponderant, with gradual effect on the NMOS threshold voltage which starts to rise again.

The other parameter change is due to sub-threshold currents which increase with dose and affect the NMOS structures. These currents are added to existing currents and are induced by parasitic structures turned on by ionization (lateral parasitic NMOS created by gate extension over field oxide, N+ source to N- substrate, etc.).

Main failures for CMOS technology and related components:

- Standby supply current increase.
- Input levels and internal noise immunity degradation, introducing functional failures.
- Increase of rise time and decrease of fall time creating change in switching and dynamic parameters.

Note: It is important to note that the irradiation conditions (dose rate, bias, temperature, etc.) highly influence the degradation. These external parameters are essential to allow a reliable prediction of radiation hardness.

Volume Effects

Heavy particles (cosmic ray, proton, electron, alpha) or high energy photons can induce volume effects. Ionization creates e-h pairs similar to current pulses in device nodes and diffusions. When these pulses reach the well (P- or N-), parasitic SCR structures inherent to CMOS topology are activated (Latch-up effect). This leads to the creation of a low resistivity path between V_{DD} and V_{SS}. The high current flowing through this path can lead to thermal destruction of the component.

When this pulse appears in a depleted zone (drain of the transistor in the off-state mode), a collection phenomenon occurs and creates a soft-error or bit-flip (state change in memory or flip-flop cells). For CMOS technology, NMOS is more sensitive than PMOS. Moreover, the electrical charge required for the cell flip decreases with scaling down of basic geometry.

Neutrons and EMP

Nuclear interaction involving neutrons is twofold:

- Atom dislocation and nuclear displacement
- Reduction of minority carrier lifetime and mobility

These two degradation mechanisms affect mainly Bipolar technologies. However, significant degradation is observed for MOS devices at neutron fluency in excess of 10^{15} neutrons/cm².

Electromagnetic pulses (EMP) generate high currents and voltages in all conductors and electronics. Counter measures against this phenomenon include box and hardware shielding.

Radiation Hardening Process Development Programs

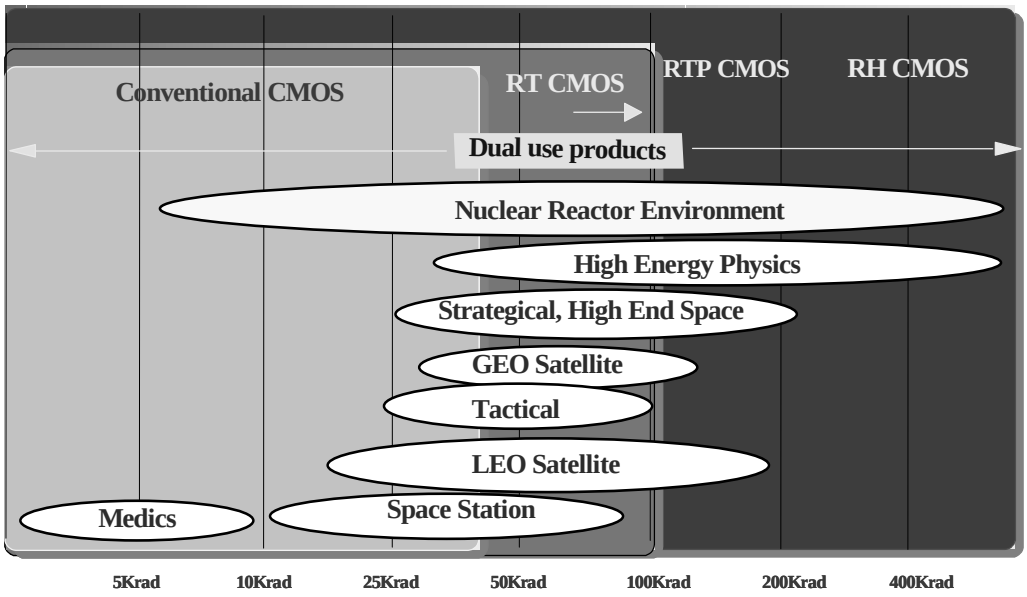
Even though CMOS and BiCMOS technology are naturally hardened against radiation, their tolerance levels are not always compatible with the Military or Space requirements.

Supported by National and European Space agencies, Atmel has, since 1986, conducted ongoing programs to harden Military and Space circuits against radiation. All research conducted is based on Dual Use policy. This concept allows developers to keep the masks sets identical for the standard and the Radiation Tolerant (RT or hadened) versions with no Design rule change. Thus, the Military and Space products benefit from the high-volume production advantages, i.e., statistical process control,

learning curve, etc. Moreover, by using ultimate technology, Atmel offers to designer and equipment manufacturers tomorrow's high performance solutions.

Moving gradually from its 3 µm CMOS technology, Atmel is now proposing a 0.18 µm, 5-metal layer CMOS, and the R&D team is studying a 0.13 µm, 6-metal layer CMOS technology to be made available in production in late 2006.

Figure 1. Technology versus Application



To cope with radiation tolerance requirements, Atmel offers a large selection of reliable technology. Depending on the requirement, either standard (soft) or radiation hard versions of CMOS technology are available. All hardened versions have improved tolerance against both long term Total Dose degradation and Heavy ion induced effects (Latch-up). Radiation Hard (RH) versions, for deep sub-micronic technologies, offer solutions to all applications above 100 Krad(Si) range total dose requirements, as they become more radiation hardened thanks to their thinner oxydes.

Hardening by Design

The hardness of a circuit is due not only to process hardness but can also be improved by DESIGN or LAYOUT techniques. There are so many techniques suitable for radiation hardness without consequence on the technology that obviously, one can't review all of them. However, this section emphasizes two of these techniques which have proven themselves at Atmel and which are currently offered to designers by Atmel.

Total Dose

Most Space and Military products are based on ASIC or ASSP approaches. This is achieved through gate array or standard cell library developments. To be able to guarantee postrad functionality to equipment manufacturers, Atmel has developed a particular methodology based on ionization induced degradation modeling which leads to a set of hardened cells suitable for either gate array or full custom (std. cell library) designs. Weakest element of the standard libraries are removed and replaced by hardened designs. Then, the designer has the option to simulate his netlist with dose and can verify timing and behavior compatibility.

Single Event Effects

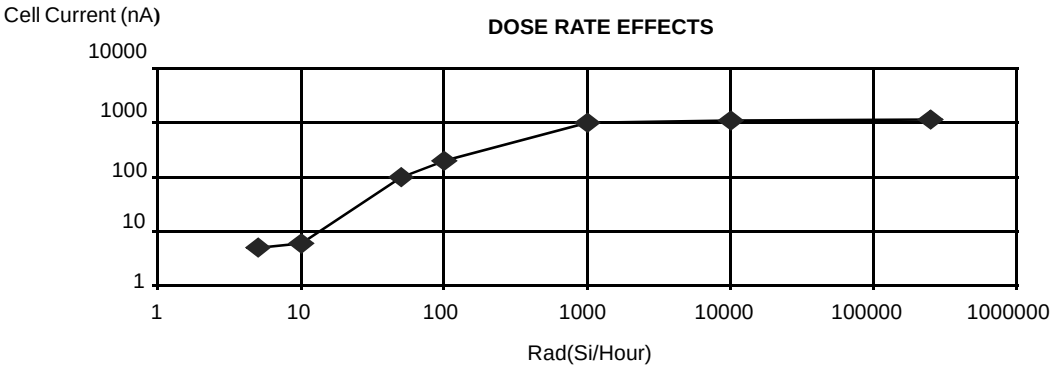
The usual way to harden circuits against heavy ion induced effects is to fix them through dedicated technologies (SOS, SOI, etc.). This has been demonstrated to be a non cost effective solution. Atmel offers several other scenarios which permit the designer to achieve hardening with limited penalties:

- Sea of Gate libraries include several flip-flop cells with different sensitivity. Depending on the application needs, LET threshold can be varied at V_{DD} = 2.7V from 15 MeV/(mg/cm²) up to total immunity. Because the technology and the layout remain the same, the penalty is minimized (only additional transistors are necessary).
- On-chip detection mechanism can also be used to harden circuits against heavy ions. Either by using parity bit checks, or any other system able to provide error notices to the external environment. Then, the single event effect has to be treated at the system level, by specific traps or interruptions handling.

Low Dose Rate Irradiation

Obviously, because of time and budget constraints, it is not possible to simulate the real use of the components in their normal environment. For that purpose, standards exist with accelerated test conditions.

But, existing dose rates proposed by either MIL std. or ESA/SCC systems are far from what the components receive in the natural space environment. The degradations which are observed are not representative of what will really occur.



Atmel and the French space agency (CNES) have conducted a dose rate study on Atmel parts. This clearly demonstrates negative effects induced by high dose rates on sensitive parameters such as leakage currents. For instance, after irradiation up to

40 Krad(Si), a standard memory cell leaks 1µA at 100 Krad(Si)/hour and 5 nA at 10 rad (Si)/hour dose rate.

Radiation Hardness Testing

Any market introduction of a new technology or real product requires from the manufacturer a lot of quite expensive testing. This is true for all necessary reliability tests (i.e., early and long term reliability figures, oxide integrity, electromigration, hot carrier degradation mechanism, etc.).

Ionization does not generally induce well understood failure mechanisms. Charge trapping, generation interface states have no direct electrical indicators. However, degradation is strongly related to oxide purity, thickness, and also to bird's beak structures. The FMEA analysis are realized to control the main contributors or to point out the main detractors of the RT processes. To monitor the quality and stability of the technology over the production time frame, Atmel has introduced, as part of the radiation hardness assurance, SPC based controls for features responsible for the radiation hardening of the technology.

For any applications with radiation tolerance requirements, it is mandatory to have some specific verifications. Rules and procedures for radiation testing are standardized (e.g. MIL system, ESA/SCC system, etc.) and we make all our total dose and heavy ion characterizations according to the standards.

Total Dose Test

According to the standards, we have set up a CO^{60} irradiation facility which allows large variations of dose rate and exposure duration. Dosimetry is regularly verified and a new source is procured this year. Static and dynamic biasing during irradiation are available and dedicated radiation test plans can be negotiated.

Electrical measurements are done using production test programs with full test coverage and datalog possibility.

Heavy Ion Test

Sensitivity against heavy ions is measured for all new designs and technologies. Heavy ion induced LATCH-UP (SEL) and Single Event Upsets (SEU) are characterized to provide reliable data to customers. These data can be further used to compute the event rate in a application.

Heavy ion accelerators are used to characterize the products over the standard Linear Energy Transfer (LET) range of the space environment.

RHA

Atmel has received, as part of their QML certification, an extension to the Radiation Hardness Assurance which is currently being implemented on products.

Reporting

Individual radiation test reports are issued for any new product family or on a case by case basis if necessary.

rning curve and similarity rules can be used to assess specific reliability figures.

Conclusions

To answer to a continually increasing requirement for satellite performance, Atmel has set up, from the start, a Dual use strategy to conserve the Electrical and Topological rules similar to those of standard technologies. This compatibility renders the Radiation Tolerant version very attractive to customers because of the performance and time to market capabilities while fulfilling almost high-end radiation requirements.

Starting from 3 µm CMOS technology, Atmel now offers state-of-the-art CMOS technologies (0.18 µm, 5-metal layers and tomorrow 0.13 µm, 6-metal layers).

Minor changes in process steps harden the technology at the level of all the space application requirements (100 Krad(Si) minimum and latch-up free at 70 $MeV.mg^{-1}.cm^2$). Using such technology modifications, Atmel has explored complementary solutions to improve product tolerance by design techniques. Thus, an ASIC hardened library including SEU free cells, as well as radiation modelization are proposed.

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