

MIPS® DSP ASE Instruction Set Quick Reference

Rd, Rs, Rt
AC
C, CC
POS, SIZE
±
∅
×
◎ / •
® / []
L/R
LL, LR, RL, RR
||
..
R2

- DESTINATION (Rd) AND SOURCE (Rs, Rt) REGISTERS
- ACCUMULATOR REGISTER (Ac0 – Ac3)
- CARRY (BIT 13) AND CONDITION CODE FLAGS (BITS 24-27) IN DSPCONTROL REGISTER
- POSITION AND SIZE (SCOUNT) FIELDS IN DSPCONTROL REGISTER
- SIGNED OPERAND/OPERATION OR SIGN EXTENSION
- UNSIGNED OPERAND/OPERATION OR ZERO EXTENSION
- INTEGER MULTIPLICATION
- FRACTIONAL MULTIPLICATION (IMPLIED SHIFT LEFT BY 1 BIT) WITH / WITHOUT ROUNDING
- ROUNDING AND SATURATION OPERATIONS
- LEFT / RIGHT 16-BIT PART OF A RESULT OR A REGISTER
- THE FOUR BYTES IN A 32-BIT REGISTER, FROM LEFT (MSB) TO RIGHT (LSB)
- BOUNDARY BETWEEN TWO OR FOUR SIMD ELEMENTS IN A REGISTER
- CONCATENATION OF BIT FIELDS
- DSP ASE REVISION 2 INSTRUCTION

ARITHMETIC OPERATIONS: 8-BIT DATA

| | | | |
|--------------------------|------------|---|-------------------------------|
| ABSQ_S.QB ^{R2} | Rd, Rs | $R_{DXY} = [R_{SXY}]$ | $XY \in \{ LL, LR, RL, RR \}$ |
| ADDU.QB | Rd, Rs, Rt | $R_{DXY} = R_{SXY}^\phi + R_{TXY}^\phi$ | $XY \in \{ LL, LR, RL, RR \}$ |
| ADDU_S.QB | Rd, Rs, Rt | $R_{DXY} = [R_{SXY}^\phi + R_{TXY}^\phi]$ | $XY \in \{ LL, LR, RL, RR \}$ |
| ADDUH.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = (R_{SXY}^\phi + R_{TXY}^\phi) \gg 1$ | $XY \in \{ LL, LR, RL, RR \}$ |
| ADDUH_R.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = (R_{SXY}^\phi + R_{TXY}^\phi + 1^\phi) \gg 1$ | $XY \in \{ LL, LR, RL, RR \}$ |
| RADDU.W.QB | Rd, Rs | $R_D = R_{SLL}^\phi + R_{SLR}^\phi + R_{SRL}^\phi + R_{RR}^\phi$ | |
| REPL.QB | Rd, CONST8 | $R_D = \text{CONST8} \parallel \text{CONST8} \parallel \text{CONST8} \parallel \text{CONST8}$ | |
| REPLV.QB | Rd, Rs | $R_D = R_{S7.0} \parallel R_{S7.0} \parallel R_{S7.0} \parallel R_{S7.0}$ | |
| SUBU.QB | Rd, Rs, Rt | $R_{DXY} = R_{SXY}^\phi - R_{TXY}^\phi$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SUBU_S.QB | Rd, Rs, Rt | $R_{DXY} = [R_{SXY}^\phi - R_{TXY}^\phi]$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SUBUH.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = (R_{SXY}^\phi - R_{TXY}^\phi) \gg 1$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SUBUH_R.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = (R_{SXY}^\phi - R_{TXY}^\phi + 1^\phi) \gg 1$ | $XY \in \{ LL, LR, RL, RR \}$ |

SHIFT OPERATIONS: 8-BIT DATA

| | | | |
|--------------------------|----------------|--|-------------------------------|
| SHLL.QB | Rd, Rs, SHIFT3 | $R_{DXY} = R_{SXY} \ll \text{SHIFT3}$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SHLLV.QB | Rd, Rs, Rt | $R_{DXY} = R_{SXY} \ll R_{T2.0}$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SHRA.QB ^{R2} | Rd, Rs, SHIFT3 | $R_{DXY} = R_{SXY}^\pm \gg \text{SHIFT3}$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SHRA_R.QB ^{R2} | Rd, Rs, SHIFT3 | $R_{DXY} = @((R_{SXY}^\pm \gg \text{SHIFT3}))$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SHRAV.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = R_{SXY}^\pm \gg R_{T2.0}$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SHRAV_R.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = @((R_{SXY}^\pm \gg R_{T2.0}))$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SHRL.QB | Rd, Rs, SHIFT3 | $R_{DXY} = R_{SXY}^\phi \gg \text{SHIFT3}$ | $XY \in \{ LL, LR, RL, RR \}$ |
| SHRLV.QB | Rd, Rs, Rt | $R_{DXY} = R_{SXY}^\phi \gg R_{T2.0}$ | $XY \in \{ LL, LR, RL, RR \}$ |

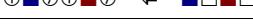
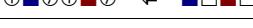
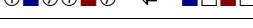
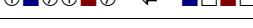
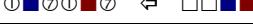
UNSIGNED INTEGER MULTIPLY OPERATIONS: 8-BIT/16-BIT DATA » GPR

| | | | |
|----------------|------------|---|--|
| MULEU_S.PH.QBL | Rd, Rs, Rt | $R_D = [R_{SLL}^\phi \times R_{TLL}^\phi]_R \parallel [R_{SLR}^\phi \times R_{TRL}^\phi]_R$ |    |
| MULEU_S.PH.QBR | Rd, Rs, Rt | $R_D = [R_{SLR}^\phi \times R_{TRL}^\phi]_R \parallel [R_{SRR}^\phi \times R_{TRR}^\phi]_R$ |    |

UNSIGNED INTEGER MULTIPLY OPERATIONS: 8-BIT DATA » ACCUMULATOR

| | | | |
|------------|------------|---|---|
| DPAU.H.QBL | Ac, Rs, Rt | $Ac += (R_{SLL}^\phi \times R_{TLL}^\phi) + (R_{SLR}^\phi \times R_{TRL}^\phi)$ |    |
| DPAU.H.QBR | Ac, Rs, Rt | $Ac += (R_{SLR}^\phi \times R_{TRL}^\phi) + (R_{SRR}^\phi \times R_{TRR}^\phi)$ |    |
| DPSU.H.QBL | Ac, Rs, Rt | $Ac -= (R_{SLL}^\phi \times R_{TLL}^\phi) + (R_{SLR}^\phi \times R_{TRL}^\phi)$ |    |
| DPSU.H.QBR | Ac, Rs, Rt | $Ac -= (R_{SLR}^\phi \times R_{TRL}^\phi) + (R_{SRR}^\phi \times R_{TRR}^\phi)$ |    |

PRECISION EXPANSION (DATA UNPACKING) OPERATIONS: 8-BIT DATA

| | | | |
|-----------------|--------|---|---|
| PRECEQU.PH.QBL | Rd, Rs | $R_D = (R_{SLL} \ll 7) \parallel (R_{SLR} \ll 7)$ |    |
| PRECEQU.PH.QBLA | Rd, Rs | $R_D = (R_{SLL} \ll 7) \parallel (R_{SRL} \ll 7)$ |    |
| PRECEQU.PH.QBR | Rd, Rs | $R_D = (R_{SLR} \ll 7) \parallel (R_{SRR} \ll 7)$ |    |
| PRECEQU.PH.QBRA | Rd, Rs | $R_D = (R_{SRL} \ll 7) \parallel (R_{SRR} \ll 7)$ |    |
| PRECEU.PH.QBL | Rd, Rs | $R_D = 0^8 \parallel R_{SLL} \parallel 0^8 \parallel R_{SLR}$ |    |
| PRECEU.PH.QBLA | Rd, Rs | $R_D = 0^8 \parallel R_{SLL} \parallel 0^8 \parallel R_{SRL}$ |    |
| PRECEU.PH.QBR | Rd, Rs | $R_D = 0^8 \parallel R_{SRL} \parallel 0^8 \parallel R_{SRR}$ |    |
| PRECEU.PH.QBRA | Rd, Rs | $R_D = 0^8 \parallel R_{SLL} \parallel 0^8 \parallel R_{SRR}$ |    |

COMPARE AND PICK OPERATIONS: 8-BIT DATA

| | | | |
|----------------------------|------------|--|-------------------------------|
| CMPGDU.EQ.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = CC_{XY} = (R_{SXY}^\phi = R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| CMPGDU.LT.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = CC_{XY} = (R_{SXY}^\phi < R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| CMPGDU.LE.QB ^{R2} | Rd, Rs, Rt | $R_{DXY} = CC_{XY} = (R_{SXY}^\phi \leq R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| CMPGU.EQ.QB | Rd, Rs, Rt | $R_{DXY} = (R_{SXY}^\phi = R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| CMPGU.LT.QB | Rd, Rs, Rt | $R_{DXY} = (R_{SXY}^\phi < R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| CMPGU.LE.QB | Rd, Rs, Rt | $R_{DXY} = (R_{SXY}^\phi \leq R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| CMPU.EQ.QB | Rd, Rs, Rt | $CC_{XY} = (R_{SXY}^\phi = R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| CMPU.LT.QB | Rd, Rs, Rt | $CC_{XY} = (R_{SXY}^\phi < R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| CMPU.LE.QB | Rd, Rs, Rt | $CC_{XY} = (R_{SXY}^\phi \leq R_{TXY}^\phi) ? 1 : 0$ | $XY \in \{ LL, LR, RL, RR \}$ |
| PICK.QB | Rd, Rs, Rt | $R_{DXY} = CC_{XY} ? R_{SXY} : R_{TXY}$ | $XY \in \{ LL, LR, RL, RR \}$ |

COMPARE AND PICK OPERATIONS: 16-BIT DATA

| | | | |
|-----------|------------|--|--|
| CMP.EQ.PH | Rd, Rs, Rt | $CC = ((R_{S_L^\pm} = R_{T_L^\pm}) ? 1 : 0) \parallel ((R_{S_R^\pm} = R_{T_R^\pm}) ? 1 : 0)$ | |
| CMP.LT.PH | Rd, Rs, Rt | $CC = ((R_{S_L^\pm} < R_{T_L^\pm}) ? 1 : 0) \parallel ((R_{S_R^\pm} < R_{T_R^\pm}) ? 1 : 0)$ | |
| CMP.LE.PH | Rd, Rs, Rt | $CC = ((R_{S_L^\pm} \leq R_{T_L^\pm}) ? 1 : 0) \parallel ((R_{S_R^\pm} \leq R_{T_R^\pm}) ? 1 : 0)$ | |
| PICK.PH | Rd, Rs, Rt | $R_D = (CC_L ? R_{S_L} : R_{T_L}) \parallel (CC_R ? R_{S_R} : R_{T_R})$ | |

| ARITHMETIC OPERATIONS: 16-BIT DATA | | |
|------------------------------------|-------------|--|
| ABSQ_S.PH | Rd, Rs | $RD = [RS_L^{\pm}] \parallel [RS_R^{\pm}]$ |
| ADDQ.PH | Rd, Rs, RT | $RD = (RS_L^{\pm} + RT_L^{\pm}) \parallel (RS_R^{\pm} + RT_R^{\pm})$ |
| ADDQ_S.PH | Rd, Rs, RT | $RD = [RS_L^{\pm} + RT_L^{\pm}] \parallel [RS_R^{\pm} + RT_R^{\pm}]$ |
| ADDQH.PH ^{R2} | Rd, Rs, RT | $RD = ((RS_L^{\pm} + RT_L^{\pm}) \gg 1) \parallel ((RS_R^{\pm} + RT_R^{\pm}) \gg 1)$ |
| ADDQH_R.PH ^{R2} | Rd, Rs, RT | $RD = @((RS_L^{\pm} + RT_L^{\pm}) \gg 1) \parallel @((RS_R^{\pm} + RT_R^{\pm}) \gg 1)$ |
| ADDU.PH ^{R2} | Rd, Rs, RT | $RD = (RS_L^{\emptyset} + RT_L^{\emptyset}) \parallel (RS_R^{\emptyset} + RT_R^{\emptyset})$ |
| ADDU_S.PH ^{R2} | Rd, Rs, RT | $RD = [RS_L^{\emptyset} + RT_L^{\emptyset}] \parallel [RS_R^{\emptyset} + RT_R^{\emptyset}]$ |
| REPL.PH | Rd, CONST10 | $RD = CONST10^{\pm} \parallel CONST10^{\pm}$ |
| REPLV.PH | Rd, Rs | $RD = RS_{15:0} \parallel RS_{15:0}$ |
| SUBQ.PH | Rd, Rs, RT | $RD = (RS_L^{\pm} - RT_L^{\pm}) \parallel (RS_R^{\pm} - RT_R^{\pm})$ |
| SUBQ_S.PH | Rd, Rs, RT | $RD = [RS_L^{\pm} - RT_L^{\pm}] \parallel [RS_R^{\pm} - RT_R^{\pm}]$ |
| SUBQH.PH ^{R2} | Rd, Rs, RT | $RD = ((RS_L^{\pm} - RT_L^{\pm}) \gg 1) \parallel ((RS_R^{\pm} - RT_R^{\pm}) \gg 1)$ |
| SUBQH_R.PH ^{R2} | Rd, Rs, RT | $RD = @((RS_L^{\pm} - RT_L^{\pm}) \gg 1) \parallel @((RS_R^{\pm} - RT_R^{\pm}) \gg 1)$ |
| SUBU.PH ^{R2} | Rd, Rs, RT | $RD = (RS_L^{\emptyset} - RT_L^{\emptyset}) \parallel (RS_R^{\emptyset} - RT_R^{\emptyset})$ |
| SUBU_S.PH ^{R2} | Rd, Rs, RT | $RD = [RS_L^{\emptyset} - RT_L^{\emptyset}] \parallel [RS_R^{\emptyset} - RT_R^{\emptyset}]$ |

| SHIFT OPERATIONS: 16-BIT DATA | | |
|-------------------------------|----------------|--|
| SHLL.PH | Rd, Rs, SHIFT4 | $RD = (RS_L \ll SHIFT4) \parallel (RS_R \ll SHIFT4)$ |
| SHLL_S.PH | Rd, Rs, SHIFT4 | $RD = [RS_L \ll SHIFT4] \parallel [RS_R \ll SHIFT4]$ |
| SHLLV.PH | Rd, Rs, RT | $RD = (RS_L \ll RT_{3:0}) \parallel (RS_R \ll RT_{3:0})$ |
| SHLLV_S.PH | Rd, Rs, RT | $RD = [RS_L \ll RT_{3:0}] \parallel [RS_R \ll RT_{3:0}]$ |
| SHRA.PH | Rd, Rs, SHIFT4 | $RD = (RS_L^{\pm} \gg SHIFT4) \parallel (RS_R^{\pm} \gg SHIFT4)$ |
| SHRA_R.PH | Rd, Rs, SHIFT4 | $RD = @((RS_L^{\pm} \gg SHIFT4)) \parallel @((RS_R^{\pm} \gg SHIFT4))$ |
| SHRAV.PH | Rd, Rs, RT | $RD = (RS_L^{\pm} \gg RT_{3:0}) \parallel (RS_R^{\pm} \gg RT_{3:0})$ |
| SHRAV_R.PH | Rd, Rs, RT | $RD = @((RS_L^{\pm} \gg RT_{3:0})) \parallel @((RS_R^{\pm} \gg RT_{3:0}))$ |
| SHRL.PH ^{R2} | Rd, Rs, SHIFT4 | $RD = (RS_L^{\emptyset} \gg SHIFT4) \parallel (RS_R^{\emptyset} \gg SHIFT4)$ |
| SHRLV.PH ^{R2} | Rd, Rs, RT | $RD = [RS_L^{\emptyset} \gg RT_{3:0}] \parallel [RS_R^{\emptyset} \gg RT_{3:0}]$ |

| PRECISION REDUCTION (DATA PACKING) OPERATIONS: 16-BIT DATA | | |
|--|------------|--|
| PRECR.QB.PH ^{R2} | Rd, Rs, RT | $RD = RS_{LR} \parallel RS_{RR} \parallel RT_{LR} \parallel RT_{RR}$ |
| PRECRQ.QB.PH | Rd, Rs, RT | $RD = RS_{LL} \parallel RS_{RL} \parallel RT_{LL} \parallel RT_{RL}$ |
| PRECRQU_S.QB.PH | Rd, Rs, RT | $RD = [RS_L^{\emptyset}]_{14:7} \parallel [RS_R^{\emptyset}]_{14:7} \parallel [RT_L^{\emptyset}]_{14:7} \parallel [RT_R^{\emptyset}]_{14:7}$ |

| PRECISION EXPANSION (DATA UNPACKING) OPERATIONS: 16-BIT DATA | | |
|--|--------|--------------------|
| PRECEQ.W.PHL | Rd, Rs | $RD = RS_L \ll 16$ |
| PRECEQ.W.PHR | Rd, Rs | $RD = RS_R \ll 16$ |

| INTEGER MULTIPLY OPERATIONS: 16-BIT DATA » ACCUMULATOR | | |
|--|------------|---|
| DPA.W.PH ^{R2} | Ac, Rs, RT | $AC += (RS_L^{\pm} \times RT_L^{\pm}) + (RS_R^{\pm} \times RT_R^{\pm})$ |
| DPAX.W.PH ^{R2} | Ac, Rs, RT | $AC += (RS_L^{\pm} \times RT_R^{\pm}) + (RS_R^{\pm} \times RT_L^{\pm})$ |
| DPS.W.PH ^{R2} | Ac, Rs, RT | $AC -= (RS_L^{\pm} \times RT_L^{\pm}) + (RS_R^{\pm} \times RT_R^{\pm})$ |
| DPSX.W.PH ^{R2} | Ac, Rs, RT | $AC -= (RS_L^{\pm} \times RT_R^{\pm}) + (RS_R^{\pm} \times RT_L^{\pm})$ |
| MULSA.W.PH ^{R2} | Ac, Rs, RT | $AC += (RS_L^{\pm} \times RT_L^{\pm}) - (RS_R^{\pm} \times RT_R^{\pm})$ |

| INTEGER MULTIPLY OPERATIONS: 16-BIT DATA » GPR | | |
|--|------------|--|
| MUL.PH ^{R2} | Rd, Rs, RT | $RD = (RS_L^{\pm} \times RT_L^{\pm})_R \parallel (RS_R^{\pm} \times RT_R^{\pm})_R$ |
| MUL_S.PH ^{R2} | Rd, Rs, RT | $RD = [RS_L^{\pm} \times RT_L^{\pm}]_R \parallel [RS_R^{\pm} \times RT_R^{\pm}]_R$ |

| FRACTIONAL MULTIPLY OPERATIONS: 16-BIT DATA » GPR | | |
|---|------------|--|
| MULQ_RS.PH | Rd, Rs, RT | $RD = [RS_L^{\pm} \odot RT_L^{\pm}]_L \parallel [RS_R^{\pm} \odot RT_R^{\pm}]_L$ |
| MULQ_S.PH ^{R2} | Rd, Rs, RT | $RD = [RS_L^{\pm} \bullet RT_L^{\pm}]_L \parallel [RS_R^{\pm} \bullet RT_R^{\pm}]_L$ |
| MULEQ_S.W.PHL | Rd, Rs, RT | $RD = [RS_L^{\pm} \bullet RT_L^{\pm}]$ |
| MULEQ_S.W.PHR | Rd, Rs, RT | $RD = [RS_R^{\pm} \bullet RT_R^{\pm}]$ |

| FRACTIONAL MULTIPLY OPERATIONS: 16-BIT DATA » ACCUMULATOR | | |
|---|------------|---|
| DPAQ_S.W.PH | Ac, Rs, RT | $AC += [RS_L^{\pm} \bullet RT_L^{\pm}] + [RS_R^{\pm} \bullet RT_R^{\pm}]$ |
| DPAQX_S.W.PH ^{R2} | Ac, Rs, RT | $AC += [RS_L^{\pm} \bullet RT_R^{\pm}] + [RS_R^{\pm} \bullet RT_L^{\pm}]$ |
| DPAQX_SA.W.PH ^{R2} | Ac, Rs, RT | $AC = [AC + [RS_L^{\pm} \bullet RT_R^{\pm}] + [RS_R^{\pm} \bullet RT_L^{\pm}]]$ |
| DPSQ_S.W.PH | Ac, Rs, RT | $AC -= [RS_L^{\pm} \bullet RT_L^{\pm}] + [RS_R^{\pm} \bullet RT_R^{\pm}]$ |
| DPSQX_S.W.PH ^{R2} | Ac, Rs, RT | $AC -= [RS_L^{\pm} \bullet RT_R^{\pm}] + [RS_R^{\pm} \bullet RT_L^{\pm}]$ |
| DPSQX_SA.W.PH ^{R2} | Ac, Rs, RT | $AC = [AC - [RS_L^{\pm} \bullet RT_R^{\pm}] + [RS_R^{\pm} \bullet RT_L^{\pm}]]$ |
| MULSAQ_S.W.PH | Ac, Rs, RT | $AC += [RS_L^{\pm} \bullet RT_L^{\pm}] - [RS_R^{\pm} \bullet RT_R^{\pm}]$ |
| MAQ_S.W.PHL | Ac, Rs, RT | $AC += [RS_L^{\pm} \bullet RT_L^{\pm}]$ |
| MAQ_S.W.PHR | Ac, Rs, RT | $AC += [RS_R^{\pm} \bullet RT_R^{\pm}]$ |
| MAQ_SA.W.PHL | Ac, Rs, RT | $AC = [AC^{\pm} + [RS_L^{\pm} \bullet RT_L^{\pm}]]$ |
| MAQ_SA.W.PHR | Ac, Rs, RT | $AC = [AC^{\pm} + [RS_R^{\pm} \bullet RT_R^{\pm}]]$ |

| ACCUMULATOR EXTRACT OPERATIONS: 16-BIT DATA | | |
|---|----------------|---------------------------|
| EXTR_S.H | Rd, Ac, SHIFT5 | $RD = [AC >> SHIFT5]_R$ |
| EXTRV_S.H | Rd, Ac, RT | $RD = [AC >> RT_{4:0}]_R$ |

| DSP CONTROL REGISTER ACCESS OPERATIONS | | |
|--|------------|-------------------------------------|
| RDDSP | Rd, MASK10 | $RD = READDSPCONTROL(MASK10_{5:0})$ |
| WRDSP | Rs, MASK10 | $WRITEDSPCONTROL(MASK10_{5:0}, RS)$ |

| ARITHMETIC OPERATIONS: 32-BIT DATA | | |
|------------------------------------|------------|--|
| ABSQ_S.W | Rd, Rs | $Rd = [Rs]$ |
| ADDQ_S.W | Rd, Rs, Rt | $Rd = [Rs^{\pm} + Rt^{\pm}]$ |
| ADDQH.W ^{R2} | Rd, Rs, Rt | $Rd = (Rs^{\pm} + Rt^{\pm}) \gg 1$ |
| ADDQH_R.W ^{R2} | Rd, Rs, Rt | $Rd = @((Rs^{\pm} + Rt^{\pm}) \gg 1)$ |
| ADDSC | Rd, Rs, Rt | C::Rd = $Rs^{\emptyset} + Rt^{\emptyset}$ |
| ADDWC | Rd, Rs, Rt | $Rd = Rs^{\emptyset} + Rt^{\emptyset} + C$ |
| SUBQ_S.W | Rd, Rs, Rt | $Rd = [Rs - Rt]$ |
| SUBQH.W ^{R2} | Rd, Rs, Rt | $Rd = (Rs^{\pm} - Rt^{\pm}) \gg 1$ |
| SUBQH_R.W ^{R2} | Rd, Rs, Rt | $Rd = @((Rs^{\pm} - Rt^{\pm}) \gg 1)$ |

| SHIFT OPERATIONS: 32-BIT DATA | | |
|-------------------------------|----------------|-----------------------------------|
| SHLL_S.W | Rd, Rs, SHIFT5 | $Rd = [Rs \ll SHIFT5]$ |
| SHLLV_S.W | Rd, Rs, Rt | $Rd = [Rs \ll RT_{4:0}]$ |
| SHRA_R.W | Rd, Rs, SHIFT5 | $Rd = @((Rs^{\pm} \gg SHIFT5))$ |
| SHRAV_R.W | Rd, Rs, Rt | $Rd = @((Rs^{\pm} \gg RT_{4:0}))$ |

| FRACTIONAL MULTIPLY OPERATIONS: 32-BIT DATA » GPR | | |
|---|------------|--------------------------------------|
| MULQ_RS.W ^{R2} | Rd, Rs, Rt | $Rd = [Rs^{\pm} \odot Rt^{\pm}]_L$ |
| MULQ_S.W ^{R2} | Rd, Rs, Rt | $Rd = [Rs^{\pm} \bullet Rt^{\pm}]_L$ |

| FRACTIONAL MULTIPLY OPERATIONS: 32-BIT DATA » ACCUMULATOR | | |
|---|------------|---|
| DPAQ_SA.L.W | Ac, Rs, Rt | $Ac = [Ac^{\pm} + [Rs^{\pm} \bullet Rt^{\pm}]]$ |
| DPSQ_SA.L.W | Ac, Rs, Rt | $Ac = [Ac^{\pm} - [Rs^{\pm} \bullet Rt^{\pm}]]$ |

| INTEGER MULTIPLY OPERATIONS: 32-BIT DATA » ACCUMULATOR | | |
|--|------------|--|
| MADD ^{R2} | Ac, Rs, Rt | $Ac += Rs^{\pm} \times Rt^{\pm}$ |
| MADDU ^{R2} | Ac, Rs, Rt | $Ac += Rs^{\emptyset} \times Rt^{\emptyset}$ |
| MSUB ^{R2} | Ac, Rs, Rt | $Ac -= Rs^{\pm} \times Rt^{\pm}$ |
| MSUBU ^{R2} | Ac, Rs, Rt | $Ac -= Rs^{\emptyset} \times Rt^{\emptyset}$ |
| MULT ^{R2} | Ac, Rs, Rt | $Ac = Rs^{\pm} \times Rt^{\pm}$ |
| MULTU ^{R2} | Ac, Rs, Rt | $Ac = Rs^{\emptyset} \times Rt^{\emptyset}$ |

| PRECISION REDUCTION (DATA PACKING) OPERATIONS: 32-BIT DATA | | |
|--|----------------|---|
| PRECRQ_PH.W | Rd, Rs, Rt | $Rd = Rs_L Rt_L$ |
| PRECRQ_RS.PH.W | Rd, Rs, Rt | $Rd = @([Rs^{\pm}]_L @([Rt^{\pm}]_L$ |
| PRECR_SRA.PH.W ^{R2} | Rd, Rs, SHIFT5 | $Rd = (Rd^{\pm} \gg SHIFT5)_R (Rs^{\pm} \gg SHIFT5)_R$ |
| PRECR_SRA_R.PH.W ^{R2} | Rd, Rs, SHIFT5 | $Rd = @((Rd^{\pm} \gg SHIFT5)_R @((Rs^{\pm} \gg SHIFT5)_R$ |

| ACCUMULATOR EXTRACT OPERATIONS: 32-BIT DATA | | |
|---|----------------|------------------------------|
| EXTR.W | Rd, Ac, SHIFT5 | $Rd = (Ac \gg SHIFT5)_R$ |
| EXTR_R.W | Rd, Ac, SHIFT5 | $Rd = @((Ac \gg SHIFT5)_R$ |
| EXTR_RS.W | Rd, Ac, SHIFT5 | $Rd = @@[Ac \gg SHIFT5]_R$ |
| EXTRV.W | Rd, Ac, Rt | $Rd = (Ac \gg RT_{4:0})_R$ |
| EXTRV_R.W | Rd, Ac, Rt | $Rd = @((Ac \gg RT_{4:0})_R$ |
| EXTRV_RS.W | Rd, Ac, Rt | $Rd = @@[Ac \gg RT_{4:0}]_R$ |

| BIT-FIELD EXTRACT OPERATIONS | | |
|------------------------------|---------------|---|
| BPOSGE32 | OFF18 | IF $POS \geq 32$, $PC += OFF18^{\pm}$ |
| EXTP | Rd, Ac, SIZE5 | $Rd = AC_{POS:POS-SIZES}$ |
| EXTPDP | Rd, Ac, SIZE5 | $Rd = AC_{POS:POS-SIZES}, POS -= (SIZE5 + 1)$ |
| EXTPV | Rd, Ac, Rs | $Rd = AC_{POS:POS-RS4:0}$ |
| EXTPDPV | Rd, Ac, Rs | $Rd = AC_{POS:POS-RS4:0}, POS -= (RS4:0 + 1)$ |
| MTHLIP | Rs, Ac | $AC_{HI} = AC_{LO}, AC_{LO} = Rs, POS += 32$ |

| LOAD DATA OPERATIONS | | |
|----------------------|------------|--|
| BITREV | Rd, Rs | $Rd = RS_{0:15}$ |
| LBUX | Rd, Rs(Rt) | $Rd = MEM8(Rs + Rt)^{\emptyset}$ |
| LHX | Rd, Rs(Rt) | $Rd = MEM16(Rs + Rt)^{\pm}$ |
| LWX | Rd, Rs(Rt) | $Rd = MEM32(Rs + Rt)$ |
| MODSUB | Rd, Rs, Rt | $Rd = (Rs \neq 0) ? (Rs - RT_{7:0}) : RT_{23:8}$ |

| ACCUMULATOR OPERATIONS | | |
|------------------------|------------|---|
| MFHI | Rd, Ac | $Rd = AC_{HI}$ |
| MFLO | Rd, Ac | $Rd = AC_{LO}$ |
| MTHI | Rs, Ac | $AC_{HI} = Rs$ |
| MTLO | Rs, Ac | $AC_{LO} = Rs$ |
| SHILO | Ac, SHIFT6 | $Ac = (SHIFT6^{\pm} \geq 0) ? (Ac \gg SHIFT6^{\pm}) : (Ac \ll -SHIFT6^{\pm})$ |
| SHILOV | Ac, Rs | $Ac = (RS_{5:0}^{\pm} \geq 0) ? (Ac \gg RS_{5:0}^{\pm}) : (Ac \ll -RS_{5:0}^{\pm})$ |

| BIT-FIELD OPERATIONS | | |
|-----------------------|----------------|--|
| APPEND ^{R2} | Rd, Rs, SHIFT5 | $Rd = (Rd \ll SHIFT5) :: RS_{SHIFT5-1:0}$ |
| BALIGN ^{R2} | Rd, Rs, BPOS2 | $Rd = (Rd \ll (8 \times BPOS2)) :: (Rs \gg (32 - 8 \times BPOS2))$ |
| INSV | Rd, Rs | $Rd_{POS+SIZE-1:POS} = RS_{SIZE-1:0}$ |
| PACKRL.PH | Rd, Rs, Rt | $Rd = RS_R RT_L$ |
| PREPEND ^{R2} | Rd, Rs, SHIFT5 | $Rd = RS_{SHIFT5-1:0} :: (Rd \gg SHIFT5)$ |