Figure 2. PXA255 processor

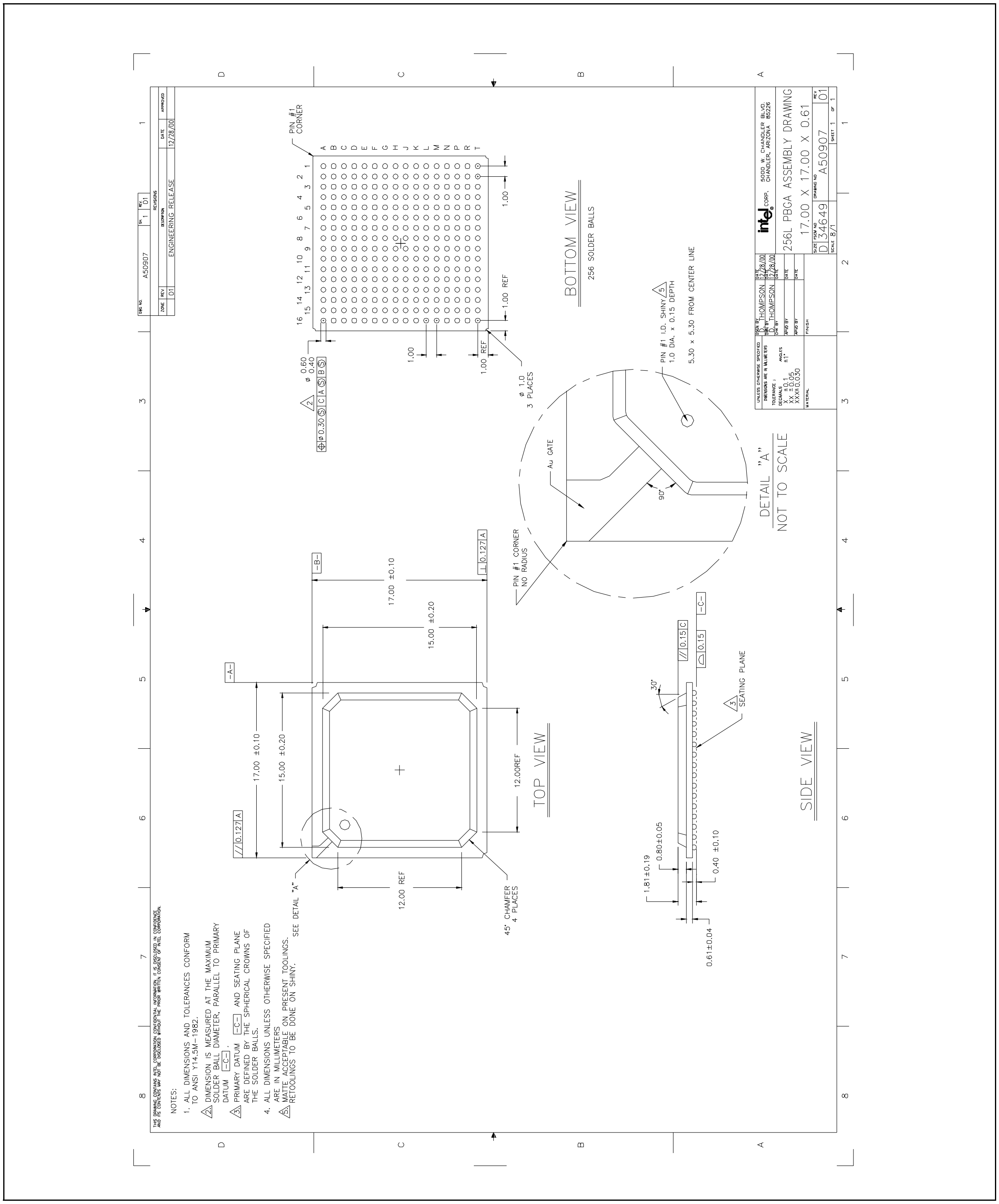

Table 5. PXA255 processor 256-Lead 17x17mm mBGA Pinout — Ballpad No. Order (Sheet 1 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	VCCN	C10	VCCQ	F3	nSDCAS
A2	L_DD[13]/GPIO[71]	C11	VSSQ	F4	VCCN
A3	L_DD[12]/GPIO[70]	C12	USB_P	F5	SDCLK[1]
A4	L_DD[11]/GPIO[69]	C13	VCCQ	F6	VSSQ
A5	L_DD[9]/GPIO[67]	C14	VSSQ	F7	GPIO[10]
A6	L_DD[7]/GPIO[65]	C15	IRTXD/GPIO[47]	F8	FFRTS/GPIO[41]
A7	GPIO[11]	C16	VSS	F9	SSPSCLK/GPIO[23]
A8	L_BIAS/GPIO[77]	D1	SDCLK[2]	F10	FFDTR/GPIO[40]
A9	SSPRXD/GPIO[26]	D2	SDCLK[0]	F11	VCC
A10	SDATA_OUT/GPIO[30]	D3	RDnWR	F12	GPIO[9]
A11	SDA	D4	VCCN	F13	BOOT_SEL[2]
A12	FFDCD/GPIO[36]	D5	L_DD[10]/GPIO[68]	F14	GPIO[8]
A13	FFRXD/GPIO[34]	D6	L_DD[5]/GPIO[63]	F15	VSSQ
A14	FFCTS/GPIO[35]	D7	L_DD[1]/GPIO[59]	F16	NSSPSCLK/GPIO[81]
A15	BTCTS/GPIO[44]	D8	L_LCLK/GPIO[75]	G1	MA[0]
A16	SDATA_IN1/GPIO[32]	D9	SSPTXD/GPIO[25]	G2	VSSN
B1	DQM[1]	D10	nACRESET	G3	nSDCS[2]
B2	DQM[2]	D11	SCL	G4	nWE
B3	L_DD[15]/GPIO[73]	D12	PWM[1]/GPIO[17]	G5	nOE
B4	GPIO[14]	D13	BTTXD/GPIO[43]	G6	nSDCS[1]
B5	GPIO[13]	D14	MMCMD	G7	VCC
B6	GPIO[12]	D15	VCCQ	G8	VSSQ
B7	L_DD[3]/GPIO[61]	D16	NSSPRXD/GPIO[84]	G9	VCC
B8	L_PCLK/GPIO[76]	E1	nSDRAS	G10	VSSQ
B9	SSPEXTCLK/GPIO[27]	E2	VSSN	G11	TESTCLK
B10	FFRI/GPIO[38]	E3	SDCKE[1]	G12	TEST
B11	FFDSR/GPIO[37]	E4	SDCKE[0]	G13	BOOT_SEL[1]
B12	USB_N	E5	L_DD[6]/GPIO[64]	G14	VCCQ
B13	BTRXD/GPIO[42]	E6	L_DD[4]/GPIO[62]	G15	GPIO[7]
B14	BTRTS/GPIO[45]	E7	L_DD[[0]/GPIO[58]	G16	BOOT_SEL[0]
B15	IRRXD/GPIO[46]	E8	L_FCLK/GPIO[74]	H1	MA[2]
B16	MMDAT	E9	SSPSFRM/GPIO[24]	H2	MA[1]
C1	RDY/GPIO[18]	E10	SDATA_IN0/GPIO[29]	H3	MD[16]
C2	VSSN	E11	SYNC/GPIO[31]	H4	VCCN
C3	L_DD[14]/GPIO[72]	E12	PWM[0]/GPIO[16]	H5	MD[17]
C4	VSSQ	E13	FFTXD/GPIO[39]	H6	MA[3]

Table 5. PXA255 processor 256-Lead 17x17mm mBGA Pinout — Ballpad No. Order (Sheet 2 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
C5	L_DD[8]/GPIO[66]	E14	VCCQ	H7	VSSQ
C6	VCCQ	E15	NSSPTXD/GPIO[83]	H8	VSS
C7	L_DD[2]/GPIO[60]	E16	NSSPSFRM/GPIO[82]	H9	VSS
C8	VSSQ	F1	nSDCS[0]	H10	VCC
C9	BITCLK/GPIO[28]	F2	nSDCS[3]	H11	nTRST
H12	TCK	L9	VCC	P6	MD[24]
H13	TMS	L10	GPIO[0]	P7	MD[26]
H14	GPIO[6]	L11	PWR_EN	P8	MD[27]
H15	TDI	L12	GPIO[1]	P9	nCS[2]/GPIO[78]
H16	TDO	L13	GPIO[2]	P10	MD[29]
J1	MA[7]	L14	VSSQ	P11	MD[12]
J2	VSSN	L15	TEXTAL	P12	MD[31]
J3	MA[6]	L16	TXTAL	P13	nPOE/GPIO[48]
J4	MD[18]	M1	MA[14]	P14	nPCE[1]/GPIO[52]
J5	MA[5]	M2	MD[21]	P15	VSSN
J6	MA[4]	M3	MA[15]	P16	nPSKTSEL/GPIO[54]
J7	VCC	M4	VCCN	R1	MA[18]
J8	VSS	M5	MD[1]	R2	VSSN
J9	VSS	M6	MD[6]	R3	MA[20]
J10	VSSQ	M7	MD[7]	R4	VSSN
J11	GPIO[5]	M8	DQM[0]	R5	MA[22]
J12	GPIO[4]	M9	MD[8]	R6	VSSN
J13	nRESET	M10	MD[15]	R7	MD[25]
J14	VSSQ	M11	VCCQ	R8	VSSN
J15	PLL_VCC	M12	GPIO[22]	R9	MD[10]
J16	PLL_VSS	M13	nPREG/GPIO[55]	R10	VSSN
K1	MA[8]	M14	VCCN	R11	MD[30]
K2	MA[9]	M15	VSSN	R12	VSSN
K3	MD[19]	M16	nIOIS16/GPIO[57]	R13	nCS[4]/GPIO[80]
K4	VCCN	N1	MD[22]	R14	VSSN
K5	MA[10]	N2	VSSN	R15	nPIOW/GPIO[51]
K6	MA[11]	N3	MA[16]	R16	nPCE[2]/GPIO[53]
K7	VSSQ	N4	MD[0]	T1	VSS
K8	VCC	N5	VCCN	T2	VCCN
K9	VSSQ	N6	MD[4]	T3	MD[23]
K10	VCC	N7	VCCN	T4	MA[21]
K11	nRESET_OUT	N8	nCS[0]	T5	MA[24]

Table 5. PXA255 processor 256-Lead 17x17mm mBGA Pinout — Ballpad No. Order (Sheet 3 of 3)

Ball #	Signal	Ball #	Signal	Ball #	Signal
K12	nBATT_FAULT	N9	VCCN	T6	MD[3]
K13	nVDD_FAULT	N10	MD[13]	T7	MD[5]
K14	GPIO[3]	N11	VCCN	T8	nCS[1]/GPIO[15]
K15	PXTAL	N12	DREQ[0]/GPIO[20]	T9	nCS[3]/GPIO[79]
K16	PEXTAL	N13	VCCN	T10	MD[9]
L1	MA[12]	N14	DREQ[1]/GPIO[19]	T11	MD[11]
L2	VSSN	N15	GPIO[21]	T12	MD[14]
L3	MA[13]	N16	nPWAIT/GPIO[56]	T13	nCS[5]/GPIO[33]
L4	MD[20]	P1	MA[17]	T14	nPWE/GPIO[49]
L5	MD[2]	P2	MA[19]	T15	nPIOR/GPIO[50]
L6	VCC	P3	VCCN	T16	VCCN
L7	DQM[3]	P4	MA[25]		
L8	MD[28]	P5	MA[23]		

3.2 Package Power Ratings

Table 6. θ_{JA} and Maximum Power Ratings

Processor	θ_{JA}	Max Power
PXA255	33 C^{O}/w	1.4W

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

This section provides the absolute maximum ratings for the processors. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.