CC1000
Single Chip Very Low Power RF Transceiver

Applications

- *Very low power UHF wireless data transmitters and receivers*
- *315 / 433 / 868 and 915 MHz ISM/SRD band systems*
- *RKE – Two-way Remote Keyless Entry*
- *Home automation*
- *Wireless alarm and security systems*
- *AMR – Automatic Meter Reading*
- *Low power telemetry*
- *Toys*

Product Description

CC1000 is a true single-chip UHF transceiver designed for very low power and very low voltage wireless applications. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency bands at 315, 433, 868 and 915 MHz, but can easily be programmed for operation at other frequencies in the 300-1000 MHz range.

The main operating parameters of **CC1000** can be programmed via an easy-to-interface serial bus, thus making **CC1000** a very flexible and easy to use transceiver. In a typical system **CC1000** will be used together with a microcontroller and a few external passive components.

CC1000 is based on Chipcon's SmartRF® technology in 0.35 µm CMOS.

Features

- True single chip UHF RF transceiver
- Very low current consumption
- Frequency range 300 – 1000 MHz
- Integrated bit synchroniser
- High sensitivity (typical -110 dBm at 2.4 kBaud)
- Programmable output power –20 to 10 dBm
- Small size (TSSOP-28 package)
- Low supply voltage (2.1 V to 3.6 V)
- Very few external components required
- No external RF switch / IF filter required
- RSSI output
- Single port antenna connection
- FSK data rate up to 76.8 kBaud
- Complies with EN 300 220 and FCC CFR47 part 15
- FSK modulation spectrum shaping
- Programmable frequency in 250 Hz steps makes crystal temperature drift compensation possible without TCXO
- Suitable for frequency hopping protocols
- Development kit available
- Easy-to-use software for generating the **CC1000** configuration data

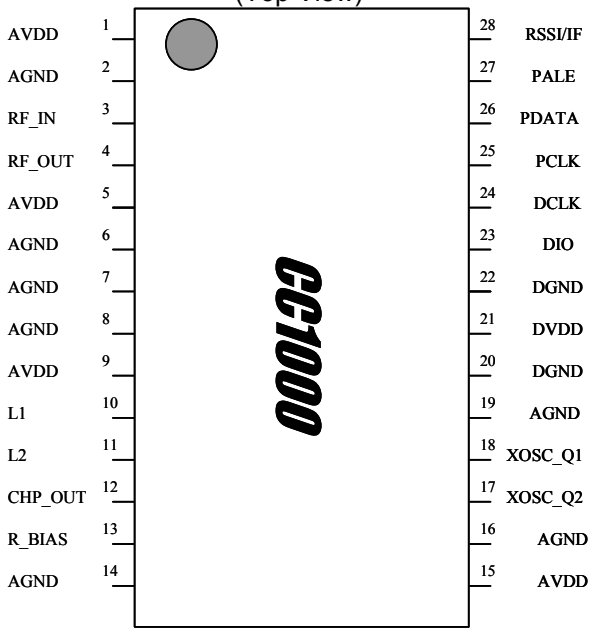
This document contains information on a pre-production product. Specifications and information herein are subject to change without notice.

Pin Assignment

Pin no.	Pin name	Pin type	Description
1	AVDD	Power (A)	Power supply (3 V) for analog modules (mixer and IF)
2	AGND	Ground (A)	Ground connection (0 V) for analog modules (mixer and IF)
3	RF_IN	RF Input	RF signal input from antenna
4	RF_OUT	RF output	RF signal output to antenna
5	AVDD	Power (A)	Power supply (3 V) for analog modules (LNA and PA)
6	AGND	Ground (A)	Ground connection (0 V) for analog modules (LNA and PA)
7	AGND	Ground (A)	Ground connection (0 V) for analog modules (PA)
8	AGND	Ground (A)	Ground connection (0 V) for analog modules (VCO and prescaler)
9	AVDD	Power (A)	Power supply (3 V) for analog modules (VCO and prescaler)
10	L1	Analog input	Connection no 1 for external VCO tank inductor
11	L2	Analog input	Connection no 2 for external VCO tank inductor
12	CHP_OUT (LOCK)	Analog output	Charge pump current output The pin can also be used as PLL Lock indicator. Output is high when PLL is in lock.
13	R_BIAS	Analog output	Connection for external precision bias resistor (82 kΩ, ± 1%)
14	AGND	Ground (A)	Ground connection (0 V) for analog modules (backplane)
15	AVDD	Power (A)	Power supply (3 V) for analog modules (general)
16	AGND	Ground (A)	Ground connection (0 V) for analog modules (general)
17	XOSC_Q2	Analog output	Crystal, pin 2
18	XOSC_Q1	Analog input	Crystal, pin 1, or external clock input
19	AGND	Ground (A)	Ground connection (0 V) for analog modules (guard)
20	DGND	Ground (D)	Ground connection (0 V) for digital modules (substrate)
21	DVDD	Power (D)	Power supply (3 V) for digital modules
22	DGND	Ground (D)	Ground connection (0 V) for digital modules
23	DIO	Digital input/output	Data input/output. Data input in transmit mode. Data output in receive mode
24	DCLK	Digital output	Data clock for data in both receive and transmit mode
25	PCLK	Digital input	Programming clock for 3-wire bus
26	PDATA	Digital input/output	Programming data for 3-wire bus. Programming data input for write operation, programming data output for read operation
27	PALE	Digital input	Programming address latch enable for 3-wire bus. Internal pull-up.
28	RSSI/IF	Analog output	The pin can be used as RSSI or 10.7 MHz IF output to optional external IF and demodulator. If not used, the pin should be left open (not connected).

A=Analog, D=Digital

(Top View)



Absolute Maximum Ratings

Parameter	Min.	Max.	Units	Condition
Supply voltage, VDD	-0.3	5.0	V	
Voltage on any pin	-0.3	VDD+0.3, max 5.0	V	
Input RF level		10	dBm	
Storage temperature range	-50	150	°C	
Operating ambient temperature range	-40	85	°C	
Lead temperature		260	°C	T = 10 s

Under no circumstances the absolute maximum ratings given above should be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

Electrical Specifications

Tc = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Overall					
RF Frequency Range	300		1000	MHz	Programmable in steps of 250 Hz
Transmit Section					
Transmit data rate	0.6		76.8	kBaud	NRZ or Manchester encoding. 76.8 kBaud equals 76.8 kbit/s using NRZ coding. See page 14.
Binary FSK frequency separation	0		65	kHz	The frequency corresponding to the digital "0" is denoted f_0, while f_1 corresponds to a digital "1". The frequency separation is f_1-f_0. The RF carrier frequency, f_c, is then given by $f_c=(f_0+f_1)/2$. (The frequency deviation is given by f_d=+/-(f_1-f_0)/2) The frequency separation is programmable in 250 Hz steps. 65 kHz is the minimum guaranteed separation at 1 MHz reference frequency. Larger separations can be achieved at higher reference frequencies.
Output power 433 MHz 868 MHz	 -20 -20		 10 5	 dBm	Delivered to 50 Ω load. The output power is programmable.
RF output impedance 433/868 MHz		140 / 80		Ω	Transmit mode. For matching details see “Input/ output matching” p.28.
Harmonics		-20		dBc	An external LC or SAW filter should be used to reduce harmonics emission to comply with SRD requirements. See p.34.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Receive Section					
Receiver Sensitivity, 433 MHz Optimum sensitivity (9.3 mA) Low current consumption (7.4 mA)		 -110 -109		 dBm	2.4 kBaud, Manchester coded data, 64 kHz frequency separation, BER = 10^{-3}
Receiver Sensitivity, 868 MHz Optimum sensitivity (11.8 mA) Low current consumption (9.6 mA)		 -107 -105		 dBm	See Table 5 and Table 6 page 19 for typical sensitivity figures at other data rates.
System noise bandwidth		30		kHz	2.4 kBaud, Manchester coded data
Cascaded noise figure 433/868 MHz		12/13		dB	
Saturation	10			dBm	2.4 kBaud, Manchester coded data, BER = 10^{-3}
Input IP3		-18		dBm	From LNA to IF output
Blocking		40		dBc	At +/- 1 MHz
LO leakage			-57	dBm	
Input impedance		 88-j26 70-j26 52-j7 52-j4		 Ω Ω Ω Ω	Receive mode, series equivalent at 315 MHz at 433 MHz at 868 MHz. at 915 MHz For matching details see “Input/ output matching” p. 28.
Turn on time	11		128	Baud	The turn-on time is determined by the demodulator settling time, which is programmable. See p. 17
IF Section					
Intermediate frequency (IF)		150	 10.7	kHz MHz	Internal IF filter External IF filter
IF bandwidth		175		kHz	
RSSI dynamic range	-105		-50	dBm	
RSSI accuracy		± 6		dB	See p.30 for details
RSSI linearity		± 2		dB	
Frequency Synthesiser Section					
Crystal Oscillator Frequency	3		16	MHz	Crystal frequency can be 3-4, 6-8 or 9-16 MHz. Recommended frequencies are 3.6864, 7.3728, 11.0592 and 14.7456. See page 32 for details.

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Crystal frequency accuracy requirement		± 50 ± 25		ppm	433 MHz 868 MHz The crystal frequency accuracy and drift (ageing and temperature dependency) will determine the frequency accuracy of the transmitted signal.
Crystal operation		Parallel			C171 and C181 are loading capacitors, see page 32
Crystal load capacitance	12 12 12	22 16 16	30 30 16	pF pF pF	3-8 MHz, 22 pF recommended 6-8 MHz, 16 pF recommended 9-16 MHz, 16 pF recommended
Crystal oscillator start-up time		5 1.5 2		ms ms ms	3.6864 MHz, 16 pF load 7.3728 MHz, 16 pF load 16 MHz, 16 pF load
Output signal phase noise		-85		dBc/Hz	At 100 kHz offset from carrier
PLL lock time (RX / TX turn time)		200		µs	Up to 1 MHz frequency step
PLL turn-on time, crystal oscillator on in power down mode		250		µs	Crystal oscillator running
Digital Inputs/Outputs					
Logic "0" input voltage	0		0.3*VDD	V	
Logic "1" input voltage	0.7*VDD		VDD	V	
Logic "0" output voltage	0		0.4	V	Output current -2.5 mA, 3.0 V supply voltage
Logic "1" output voltage	2.5		VDD	V	Output current 2.5 mA, 3.0 V supply voltage
Logic "0" input current	NA		-1	µA	Input signal equals GND
Logic "1" input current	NA		1	µA	Input signal equals VDD
DIO setup time	20			ns	TX mode, minimum time DIO must be ready before the positive edge of DCLK
DIO hold time	10			ns	TX mode, minimum time DIO must be held after the positive edge of DCLK
Serial interface (PCLK, PDATA and PALE) timing specification					See Table 2 page 12
Power Supply					
Supply voltage		3.0		V	Recommended operation voltage
	2.1		3.6	V	Operating limits
Power Down mode		0.2	1	µA	Oscillator core off
Current Consumption, receive mode 433/868 MHz		7.4/9.6		mA	Current is programmable and can be increased for improved sensitivity
Current Consumption, average in receive mode using polling 433/868 MHz		74/96		µA	Polling controlled by micro-controller using 1:100 receive to power down ratio

Parameter	Min.	Typ.	Max.	Unit	Condition / Note
Current Consumption, transmit mode 433/868 MHz:					
P=0.01mW (-20dBm)		5.3/8.6		mA	The ouput power is delivered to a 50Ω load, see also p. 29
P=0.3mW (-5dBm)		8.9/13.8		mA	
P=1mW (0dBm)		10.4/16.5		mA	
P=3mW (5dBm)		14.8/25.4		mA	
P=10mW (10dBm)		26.7/NA		mA	
Current Consumption, crystal osc.		30 80 105		µA	3-8 MHz, 16 pF load 9-14 MHz, 12 pF load 14-16 MHz, 16 pF load
Current Consumption, crystal osc. and bias		860		µA	
Current Consumption, crystal osc., bias and synthesiser, RX/TX		4/5 5/6		mA mA	< 500 MHz > 500 MHz

Circuit Description

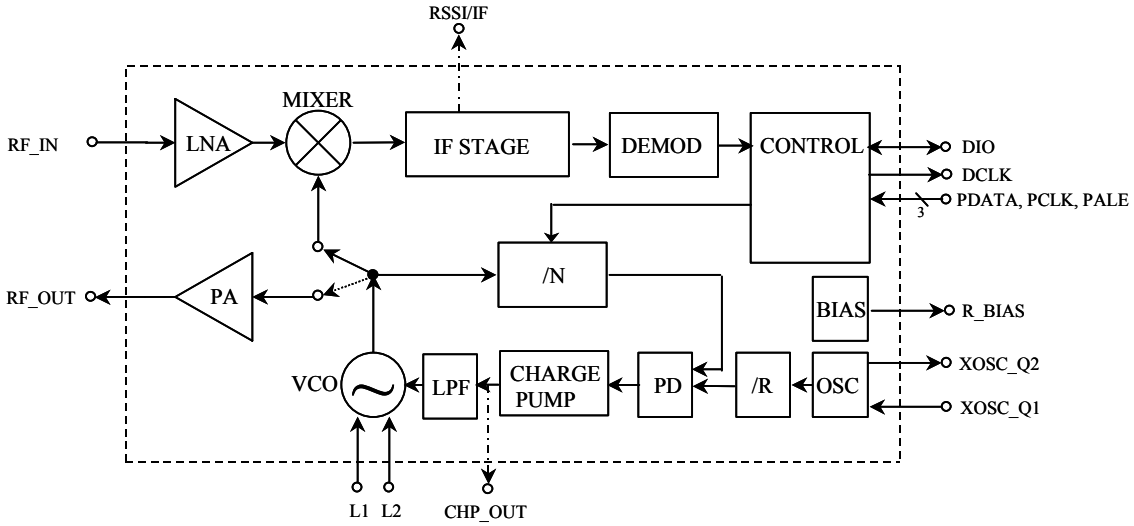


Figure 1. Simplified block diagram of the *CC1000*

A simplified block diagram of ***CC1000*** is shown in Figure 1. Only signal pins are shown.

In receive mode ***CC1000*** is configured as a traditional superheterodyne receiver. The RF input signal is amplified by the low-noise amplifier (LNA) and converted down to the intermediate frequency (IF) by the mixer (MIXER). In the intermediate frequency stage (IF STAGE) this downconverted signal is amplified and filtered before being fed to the demodulator (DEMOD). As an option a RSSI signal, or the IF signal after the mixer is available at the RSSI/IF pin. After demodulation ***CC1000*** outputs the digital demodulated data on the pin DIO. Synchronisation is done on-chip providing data clock at DCLK.

In transmit mode the voltage controlled oscillator (VCO) output signal is fed directly to the power amplifier (PA). The RF output is frequency shift keyed (FSK) by the digital bit stream fed to the pin DIO. The internal T/R switch circuitry makes the antenna interface and matching very easy.

The frequency synthesiser generates the local oscillator signal which is fed to the MIXER in receive mode and to the PA in transmit mode. The frequency synthesiser consists of a crystal oscillator (XOSC), phase detector (PD), charge pump (CHARGE PUMP), VCO, and frequency dividers (/R and /N). An external crystal must be connected to XOSC, and only an external inductor is required for the VCO.

The 3-wire digital serial interface (CONTROL) is used for configuration.

Application Circuit

Very few external components are required for the operation of ***CC1000***. A typical application circuit is shown in Figure 2. Component values are shown in Table 1.

Input / output matching
C31/L32 is the input match for the receiver, and L32 is also a DC choke for biasing. C41, L41 and C42 are used to match the transmitter to 50 Ohm. An internal T/R switch circuit makes it possible to connect the input and output together and match the ***CC1000*** to 50 Ω in both RX and TX mode. See “Input/output matching” p.28 for details.

VCO inductor
The VCO is completely integrated except for the inductor L101.

Component values for the matching network and VCO inductor are easily calculated using the SmartRF Studio software.

Additional filtering
Additional external components (e.g. RF LC or SAW-filter) may be used in order to improve the performance in specific applications. See also “Optional LC filter” p.34 for further information.

Voltage supply decoupling
C10-C16 are voltage supply de-coupling capacitors. These capacitors should be placed as close as possible to the voltage supply pins of ***CC1000***.

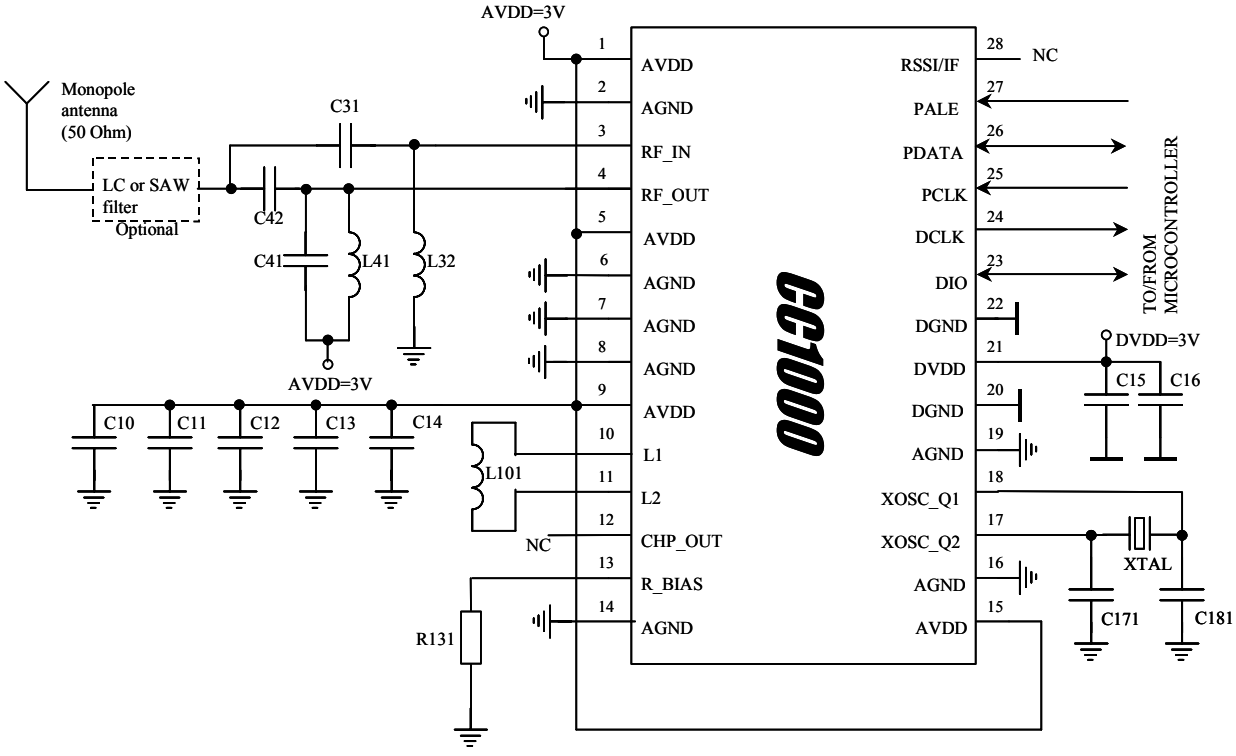


Figure 2. Typical *CC1000* application circuit

Item	315 MHz	433 MHz	868 MHz	915 MHz
C10	33 nF, 10%, X7R, 0805	33 nF, 10%, X7R, 0805	33 nF, 10%, X7R, 0805	33 nF, 10%, X7R, 0805
C11	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603
C12	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603
C13	220 pF, 10%, C0G, 0603	220 pF, 10%, C0G, 0603	220 pF, 10%, C0G, 0603	220 pF, 10%, C0G, 0603
C14	220 pF, 10%, C0G, 0603	220 pF, 10%, C0G, 0603	220 pF, 10%, C0G, 0603	220 pF, 10%, C0G, 0603
C15	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603	1 nF, 10%, X7R, 0603
C16	33 nF, 10%, X7R, 0805	33 nF, 10%, X7R, 0805	33 nF, 10%, X7R, 0805	33 nF, 10%, X7R, 0805
C31	8.2 pF, 5%, C0G, 0603	15 pF, 5%, C0G, 0603	10 pF, 5%, C0G, 0603	10 pF, 5%, C0G, 0603
C41	2.2 pF, 5%, C0G, 0603	8.2 pF, 5%, C0G, 0603	Not used	Not used
C42	5.6 pF, 5%, C0G, 0603	5.6 pF, 5%, C0G, 0603	4.7 pF, 5%, C0G, 0603	4.7 pF, 5%, C0G, 0603
C141	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603
C151	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603	18 pF, 5%, C0G, 0603
L32	39 nH, 10%, 0805 (Coilcraft 0805CS-390XKBC)	68 nH, 10%, 0805 (Coilcraft 0805CS-680XKBC)	120 nH, 10%, 0805 (Coilcraft 0805CS-121XKBC)	120 nH, 10%, 0805 (Coilcraft 0805CS-121XKBC)
L41	20 nH, 10%, 0805 (Coilcraft 0805HQ-20NXKBC)	6.2 nH, 10%, 0805 (Coilcraft 0805HQ-6N2XKBC)	2.5 nH, 10%, 0805 (Coilcraft 0805HQ-2N5XKBC)	2.5 nH, 10%, 0805 (Coilcraft 0805HQ-2N5XKBC)
L101	56 nH, 5%, 0805 (Koa KL732ATE56NJ)	33 nH, 5%, 0805 (Koa KL732ATE33NJ)	4.7 nH, 5%, 0805 (Koa KL732ATE4N7C)	4.7 nH, 5%, 0805 (Koa KL732ATE4N7C)
R131	82 kΩ, 1%, 0603	82 kΩ, 1%, 0603	82 kΩ, 1%, 0603	82 kΩ, 1%, 0603
XTAL	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load	14.7456 MHz crystal, 16 pF load

Note: Items shaded are different for different frequencies

Table 1. Bill of materials for the application circuit

Note that the component values for 868/915 MHz can be the same. However, it is important the layout is optimised for the selected VCO inductor in order to centre the tuning range around the operating frequency to account for inductor tolerance. The VCO inductor must be placed very close and symmetrical with respect to the pins (L1 and L2).

Chipcon provide reference layouts that should be followed very closely in order to achieve the best performance. The CC1000PP Plug & Play reference design can be downloaded from the Chipcon website.

Configuration Overview

CC1000 can be configured to achieve the best performance for different applications. Through the programmable configuration registers the following key parameters can be programmed:

- Receive / transmit mode
- RF output power
- Frequency synthesiser key parameters: RF output frequency, FSK frequency separation (deviation), crystal oscillator reference frequency
- Power-down / power-up mode
- Crystal oscillator power-up / power down
- Data rate and data format (NRZ, Manchester coded or UART interface)
- Synthesiser lock indicator mode
- Optional RSSI or external IF

Configuration Software

Chipcon provides users of ***CC1000*** with a software program, SmartRF Studio (Windows interface) that generates all necessary ***CC1000*** configuration data based on the user's selections of various parameters. These hexadecimal numbers will then be the necessary input to the microcontroller for the configuration of ***CC1000***. In addition the program will provide the user with the component values needed for the input/output matching circuit and the VCO inductor.

Figure 3 shows the user interface of the ***CC1000*** configuration software.

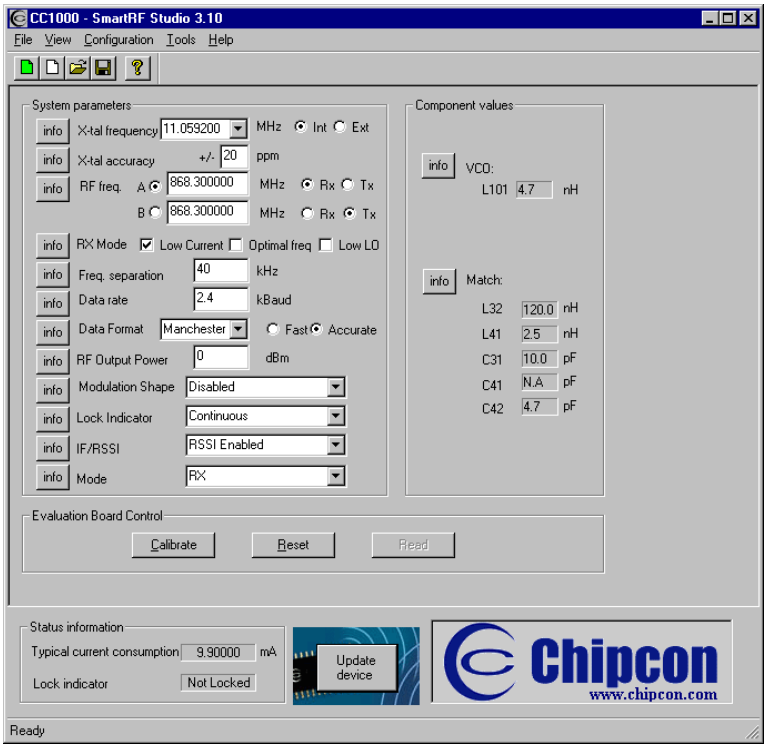


Figure 3. SmartRF Studio user interface

3-wire Serial Configuration Interface

CC1000 is configured via a simple 3-wire interface (PDATA, PCLK and PALE). There are 36 8-bit configuration registers, each addressed by a 7-bit address. A Read/Write bit initiates a read or write operation. A full configuration of ***CC1000*** requires sending 29 data frames of 16 bits each (7 address bits, R/W bit and 8 data bits). The time needed for a full configuration depend on the PCLK frequency. With a PCLK frequency of 10 MHz the full configuration is done in less than 60 μs. Setting the device in power down mode requires sending one frame only and will in this case take less than 2 μs. All registers are also readable.

In each write-cycle 16 bits are sent on the PDATA-line. The seven most significant bits of each data frame (*A6:0)* are the address-bits. *A6* is the MSB (Most Significant Bit) of the address and is sent as the first bit. The next bit is the R/W bit (high for write, low for read). During address and R/W bit transfer the PALE (Program Address Latch Enable) must be kept low. The 8 data-bits are then transferred (*D7:0*). See Figure 4.

The timing for the programming is also shown in Figure 4 with reference to Table 2. The clocking of the data on PDATA is done on the negative edge of PCLK. When the last bit, *D0*, of the 8 data-bits has been loaded, the data word is loaded in the internal configuration register.

The configuration data is stored in internal RAM. The data is retained during power-down mode, but not when the power-supply is turned off. The registers can be programmed in any order.

The configuration registers can also be read by the microcontroller via the same configuration interface. The seven address bits are sent first, then the R/W bit set low to initiate the data read-back. ***CC1000*** then returns the data from the addressed register. PDATA is in this case used as an output and must be tri-stated (or set high n the case of an open collector pin) by the microcontroller during the data read-back (D7:0). The read operation is illustrated in Figure 5.

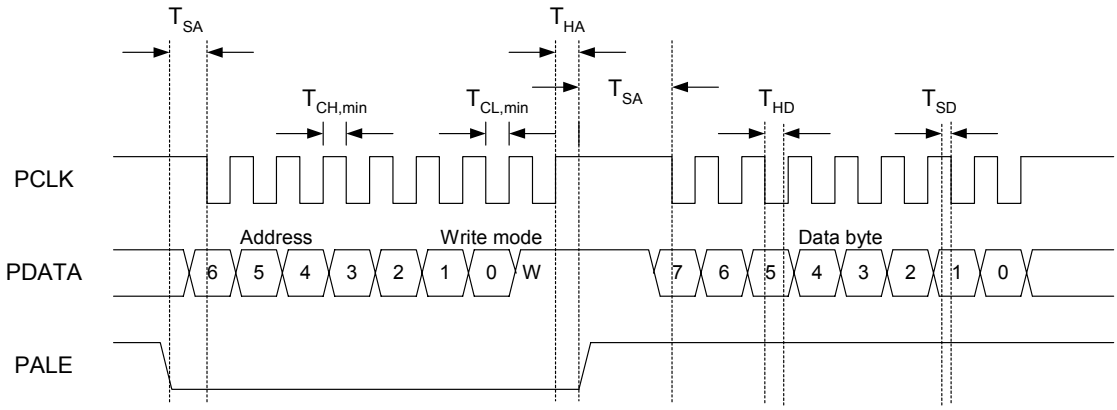


Figure 4. Configuration registers write operation

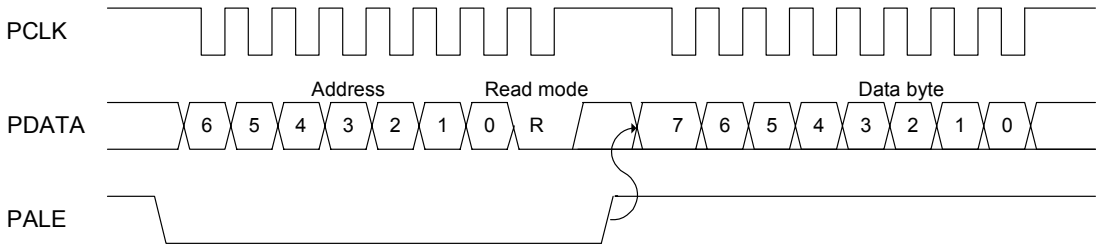


Figure 5. Configuration registers read operation

Parameter	Symbol	Min	Max	Units	Conditions
PCLK, clock frequency	F_{CLOCK}	-	10	MHz	
PCLK low pulse duration	$T_{CL,min}$	50		ns	The minimum time PCLK must be low.
PCLK high pulse duration	$T_{CH,min}$	50		ns	The minimum time PCLK must be high.
PALE setup time	T_{SA}	10	-	ns	The minimum time PALE must be low before negative edge of PCLK.
PALE hold time	T_{HA}	10	-	ns	The minimum time PALE must be held low after the *positive* edge of PCLK.
PDATA setup time	T_{SD}	10	-	ns	The minimum time data on PDATA must be ready before the negative edge of PCLK.
PDATA hold time	T_{HD}	10	-	ns	The minimum time data must be held at PDATA, after the negative edge of PCLK.
Rise time	T_{rise}		100	ns	The maximum rise time for PCLK and PALE
Fall time	T_{fall}		100	ns	The maximum fall time for PCLK and PALE

Note: The set-up- and hold-times refer to 50% of VDD.

Table 2. Serial interface, timing specification

Microcontroller Interface

Used in a typical system, **CC1000** will interface to a microcontroller. This microcontroller must be able to:

- Program **CC1000** into different modes via the 3-wire serial configuration interface (PDATA, PCLK and PALE).
- Interface to the bi-directional synchronous data signal interface (DIO and DCLK).
- Optionally the microcontroller can do data encoding / decoding.
- Optionally the microcontroller can monitor the frequency lock status from pin CHP_OUT (LOCK).
- Optionally the microcontroller can monitor the RSSI output for signal strength acquisition.

Connecting the microcontroller

The microcontroller uses 3 output pins for the configuration interface (PDATA, PCLK and PALE). PDATA should be a bi-directional pin for data read-back. A bi-directional pin is used for data (DIO) to be transmitted and data received. DCLK providing the data timing should be connected to a microcontroller input. Optionally another pin can be used to monitor the LOCK signal (available at the CHP_OUT pin). This signal is logic level high when the PLL is in lock. See Figure 6.

Also the RSSI signal can be connected to the microcontroller if it has an analogue ADC input.

The microcontroller pins connected to PDATA and PCLK can be used for other purposes when the configuration interface is not used. PDATA and PCLK are high impedance inputs as long as PALE is not activated.

PALE has an internal pull-up resistor and should be left open (tri-stated by the microcontroller) or set to a high level during power down mode in order to prevent a trickle current flowing in the pull-up.

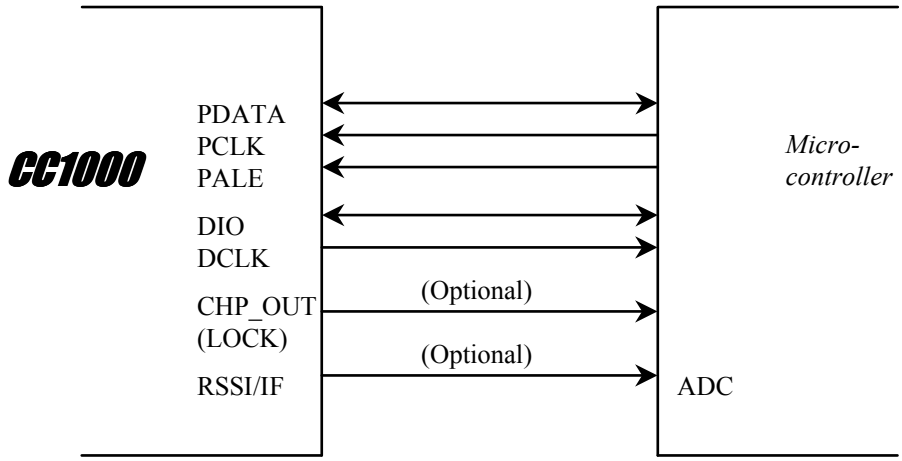


Figure 6. Microcontroller interface

Signal interface

The signal interface consists of DIO and DCLK and is used for the data to be transmitted and data received. DIO is the bi-directional data line and DCLK provides a synchronous clock both during data transmission and data reception.

The ***CC1000*** can be used with NRZ (Non-Return-to-Zero) data or Manchester (also known as bi-phase-level) encoded data. ***CC1000*** can also synchronise the data from the demodulator and provide the data clock at DCLK.

CC1000 can be configured for three different data formats:

Synchronous NRZ mode. In transmit mode ***CC1000*** provides the data clock at DCLK, and DIO is used as data input. Data is clocked into ***CC1000*** at the rising edge of DCLK. The data is modulated at RF without encoding. ***CC1000*** can be configured for the data rates 0.6, 1.2, 2.4, 4.8, 9.6, 19.2, 38.4 or 76.8 kbit/s. For 38.4 and 76.8 kbit/s a crystal frequency of 14.7456 MHz must be used. In receive mode ***CC1000*** does the synchronisation and provides received data clock at DCLK and data at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 7.

Synchronous Manchester encoded mode. In transmit mode ***CC1000*** provides the data clock at DCLK, and DIO is used as data input. Data is clocked into ***CC1000*** at the rising edge of DCLK and should be in NRZ format. The data is modulated at RF with Manchester code. The encoding is done by ***CC1000***. In this mode ***CC1000*** can be configured for the data rates 0.3, 0.6, 1.2, 2.4, 4.8, 9.6, 19.2 or 38.4 kbit/s. The 38.4 kbit/s rate corresponds to the maximum 76.8 kBaud due to the Manchester encoding. For 38.4 and 76.8 kBaud a crystal frequency of 14.7456 MHz must be used. In receive mode ***CC1000*** does the synchronisation and provides received data clock at DCLK and data at DIO. ***CC1000*** does the decoding and NRZ data is presented at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 8.

Transparent Asynchronous UART mode. In transmit mode DIO is used as data input. The data is modulated at RF without synchronisation or encoding. In receive mode the raw data signal from the demodulator is sent to the output. No synchronisation or decoding of the signal is done in ***CC1000*** and should be done by the interfacing circuit. The DCLK pin is used as data output in this mode. Data rates in the range from 0.6 to 76.8 kBaud can be used. For 38.4 and 76.8 kBaud a crystal frequency of 14.7456 MHz must be used. See Figure 9.

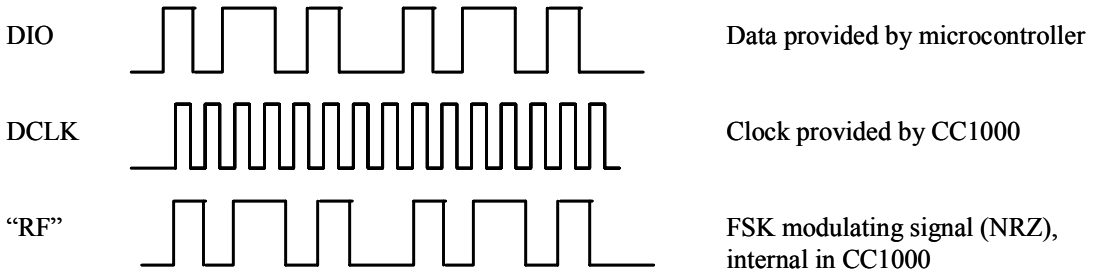
Manchester encoding and decoding

In the *Synchronous Manchester encoded mode* ***CC1000*** uses Manchester coding when modulating the data. The ***CC1000*** also performs the data decoding and synchronisation. The Manchester code is based on transitions; a “0” is encoded as a low-to-high transition, a “1” is encoded as a high-to-low transition. See Figure 10.

The ***CC1000*** can detect a Manchester decoding violation and will set a Manchester Violation Flag when such a violation is detected in the incoming signal. The threshold limit for the Manchester Violation can be set in the *MODEM1* register. The Manchester Violation Flag can be monitored at the CHP_OUT (LOCK) pin, configured in the *LOCK* register.

The Manchester code ensures that the signal has a constant DC component, which is necessary in some FSK demodulators. Using this mode also ensures compatibility with CC400/CC900 designs.

Transmitter side:



Receiver side:

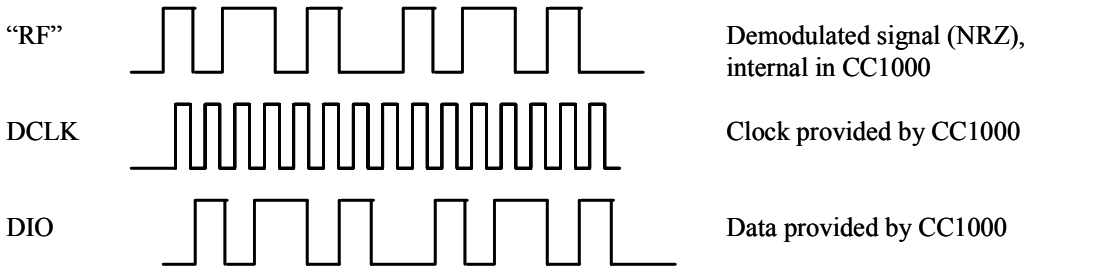
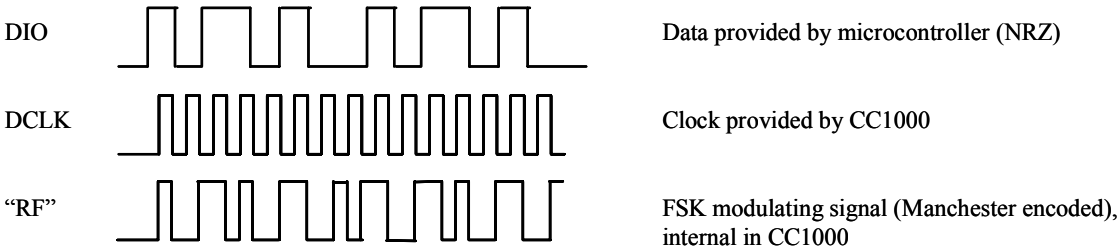


Figure 7. Synchronous NRZ mode

Transmitter side:



Receiver side:

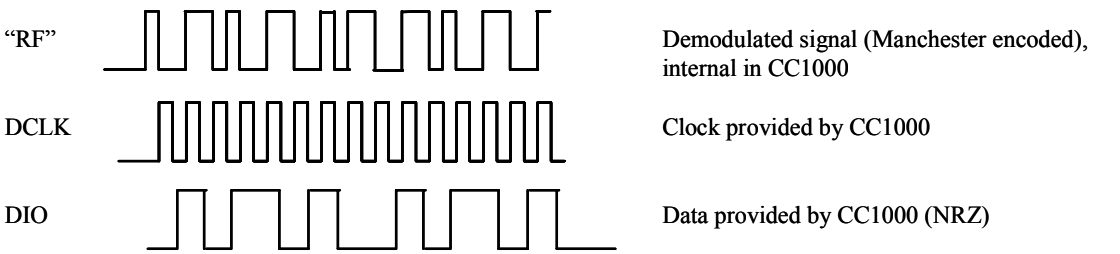
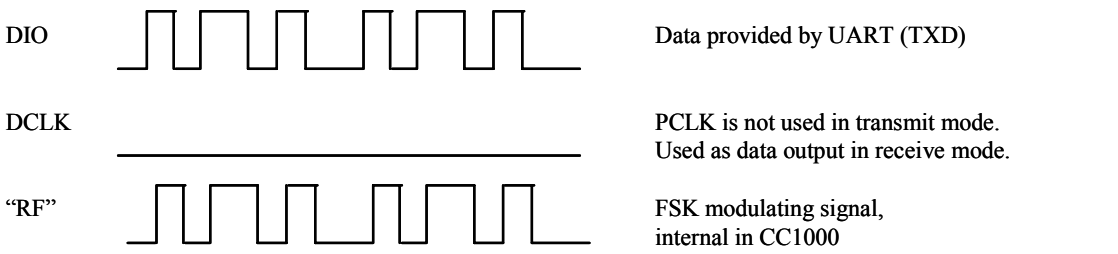


Figure 8. Synchronous Manchester encoded mode

Transmitter side:



Receiver side:

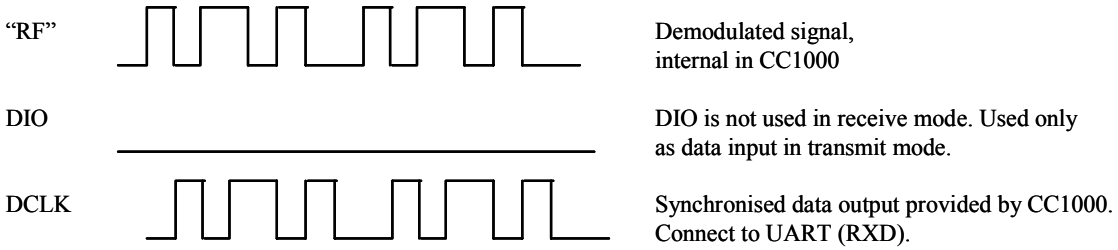


Figure 9. Transparent Asynchronous UART mode

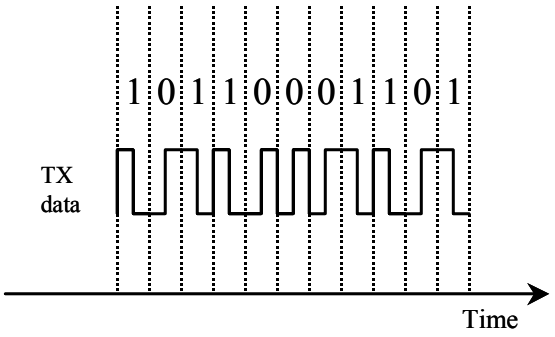


Figure 10. Manchester encoding

Bit synchroniser and data decision

The built-in bit synchroniser extracts the data rate and performs data decision. The data decision is done using over-sampling and digital filtering of the incoming signal. This improves the reliability of the data transmission. Using the synchronous modes simplifies the data-decoding task substantially.

All modes need a DC balanced preamble for the internal data slicer to acquire correct comparison level from an averaging filter. The suggested preamble is a '010101…' bit pattern. The same bit pattern should also be used in Manchester mode, giving a '011001100110…'chip' pattern. This is necessary for the bit synchronizer to synchronize correctly.

The minimum length of the preamble depends on the acquisition mode selected. The locking of the averaging filter value can be done through the configuration interface, or it can be done automatically after a predefined time (*LOCK_AVG_MODE* in *MODEM1*).

In a polled receiver system the automatic locking can be used. This is illustrated in Figure 11. If the receiver is operated continuously and searching for a preamble, the averaging filter should be locked manually as soon as the preamble is detected. This is shown in Figure 12. If the data is Manchester coded there is no need to lock the averaging filter as shown in Figure 13.

The minimum number of balanced bauds ('chips') depends on the settling time of the averaging filter which is set by *SETTLING* in *MODEM1*. Table 3 gives the minimum recommended number of chips for the preamble in NRZ and UART modes. In this context 'chips' refer to the data coding. Using Manchester coding every bit consists of two 'chips'.

If Manchester coding is used, there is no need to lock the averaging filter and it can be left free-running (*LOCK_AVG_IN* in *MODEM1*). Table 4 gives the the minimum recommended number of bauds (chips) for the preamble in Manchester mode.

Settling *SETTLING**	**Manual Lock** **NRZ mode** *LOCK_AVG_MODE* =1 *LOCK_AVG_IN = 0→1***	**Manual Lock** **UART mode** *LOCK_AVG_MODE* =1 *LOCK_AVG_IN = 0→1***	**Automatic Lock** **NRZ mode** *LOCK_AVG_MODE* =0 *LOCK_AVG_IN = X****	**Automatic Lock** **UART mode** *LOCK_AVG_MODE* =0 *LOCK_AVG_IN = X****
00	14	11	16	16
01	25	22	32	32
10	46	43	64	64
11	89	86	128	128

Notes:
*All configuration bits are in the *MODEM1* register
** The averaging filter is locked when *LOCK_AVG_IN* is set to 1
*** X = Do not care. The timer for the automatic lock is started when RX mode is set in the MAIN register

Table 3. Minimum number of balanced bauds (chips) in the preamble in NRZ and UART modes

Settling *SETTLING**	**Free-running** **Manchester mode** *LOCK_AVG_MODE* =1 *LOCK_AVG_IN = 0*
00	23
01	34
10	55
11	98

Note: *All configuration bits are in the *MODEM1* register

Table 4. Minimum number of balanced bauds (chips) in the preamble in Manchester mode

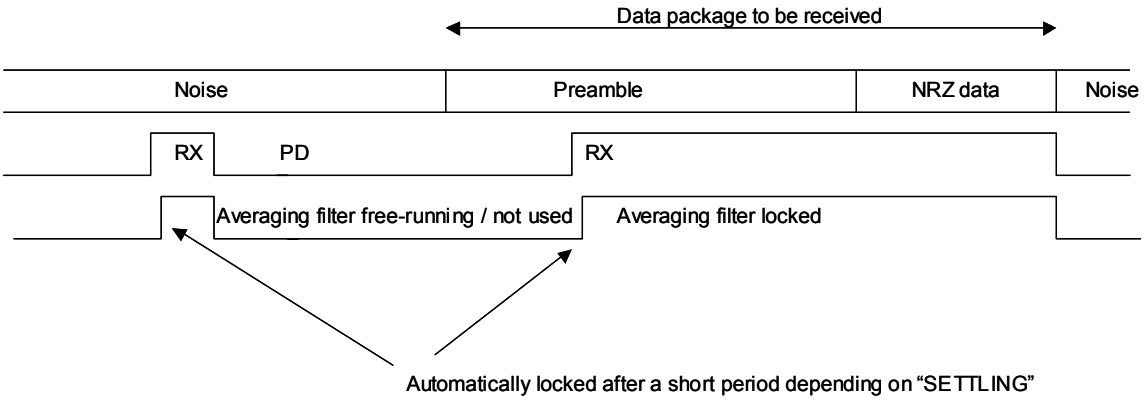


Figure 11. Automatic locking of the averaging filter

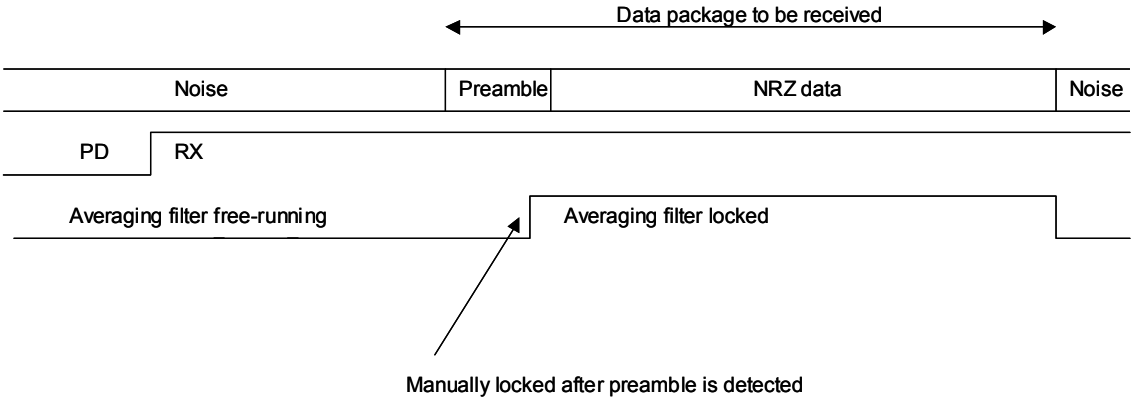


Figure 12. Manual locking of the averaging filter

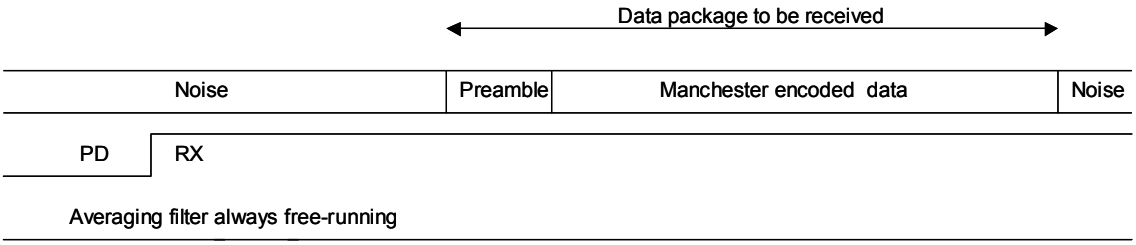


Figure 13. Free-running averaging filter

Receiver sensitivity versus data rate and frequency separation

The receiver sensitivity depends on the data rate, the data format, FSK frequency separation and the RF frequency. Typical figures for the receiver sensitivity (BER = 10^{-3}) are shown in Table 5 for 64 kHz frequency separations and Table 6 for 20 kHz. Optimised sensitivity configurations are used. For best performance the frequency separation should be as high as possible especially at high data rates. Table 7 shows the sensitivity for low current settings. See page 25 for how to program different current consumption.

Data rate [kBaud]	Separation [kHz]	433 MHz			868 MHz		
		NRZ mode	Manchester mode	UART mode	NRZ mode	Manchester mode	UART mode
0.6	64	-113	-114	-113	-110	-111	-110
1.2	64	-111	-112	-111	-108	-109	-108
2.4	64	-109	-110	-109	-106	-107	-106
4.8	64	-107	-108	-107	-104	-105	-104
9.6	64	-105	-106	-105	-102	-103	-102
19.2	64	-103	-104	-103	-100	-101	-100
38.4	64	-102	-103	-102	-98	-99	-98
76.8	64	-100	-101	-100	-97	-98	-97
Average current consumption		9.3 mA			11.8 mA		

Table 5. Receiver sensitivity as a function of data rate at 433 and 868 MHz, BER = 10^{-3}, frequency separation 64 kHz, normal current settings

Data rate [kBaud]	Separation [kHz]	433 MHz			868 MHz		
		NRZ mode	Manchester mode	UART mode	NRZ mode	Manchester mode	UART mode
0.6	20	-109	-111	-109	-106	-108	-106
1.2	20	-108	-110	-108	-104	-106	-104
2.4	20	-106	-108	-106	-103	-105	-103
4.8	20	-104	-106	-104	-101	-103	-101
9.6	20	-103	-104	-103	-100	-101	-100
19.2	20	-102	-103	-102	-99	-100	-99
38.4	20	-98	-100	-98	-98	-99	-98
76.8	20	-94	-98	-94	-94	-96	-94
Average current consumption		9.3 mA			11.8 mA		

Table 6. Receiver sensitivity as a function of data rate at 433 and 868 MHz, BER = 10^{-3}, frequency separation 20 kHz, normal current settings

Data rate [kBaud]	Separation [kHz]	433 MHz			868 MHz		
		NRZ mode	Manchester mode	UART mode	NRZ mode	Manchester mode	UART mode
0.6	64	-111	-113	-111	-107	-109	-107
1.2	64	-110	-111	-110	-106	-107	-106
2.4	64	-108	-109	-108	-104	-105	-104
4.8	64	-106	-107	-106	-102	-103	-102
9.6	64	-104	-105	-104	-100	-101	-100
19.2	64	-102	-103	-102	-98	-99	-98
38.4	64	-101	-102	-101	-96	-97	-96
76.8	64	-99	-100	-99	-95	-96	-95
Average current consumption		7.4 mA			9.6 mA		

Table 7. Receiver sensitivity as a function of data rate at 433 and 868 MHz, BER = 10^{-3}, frequency separation 64 kHz , low current settings

Frequency programming

The operation frequency is set by programming the frequency word in the configuration registers. There are two frequency words registers, termed *A* and *B*, which can be programmed to two different frequencies. One of the frequency words can be used for RX (local oscillator frequency) and other for TX (transmitting frequency) in order to be able to switch very fast between RX mode and TX mode. They can also be used for RX (or TX) at two different channels. Frequency word *A* or *B* is selected by the *F_REG* bit in the *MAIN* register.

The frequency word is 24 bits (3 bytes) located in *FREQ_2A:FREQ_1A:FREQ_0A* and *FREQ_2B:FREQ_1B:FREQ_0B* for the *A* and *B* word respectively.

The FSK frequency separation is programmed in the *FSEP1:FSEP0* registers (11 bits).

The frequency word *FREQ* is calculated by:

$$f_{VCO} = f_{ref} \cdot \frac{FREQ + 8192}{16384}$$

where the reference frequency is the crystal oscillator clock divided by *REFDIV* (4 bits in the *PLL* register), a number between 2 and 15:

$$f_{ref} = \frac{f_{xosc}}{REFDIV}$$

The equation above gives the VCO frequency, that is, f_{VCO} is the LO frequency for receive mode, and the f_0 frequency for transmit mode (lower FSK frequency).

The upper FSK frequency is given by:
$f_1 = f_0 + f_{sep}$
where f_{sep} is set by the separation word:

$$f_{sep} = f_{ref} \cdot \frac{FSEP}{16384}$$

Recommended settings for ISM frequencies

Shown in Table 8 are the recommended frequency synthesiser settings for a few operating frequencies in the popular ISM bands. These settings ensure optimum configuration of the synthesiser in receive mode for best sensitivity. For some settings of the synthesiser (combinations of RF frequencies and reference frequency), the receiver sensitivity is degraded. The performance of the transmitter is not affected by the settings, but recommended transmitter settings are included for completeness. The FSK frequency separation is set to 64 kHz. The SmartRF Studio can be used to generate optimised configuration data as well. Also an application note (AN011) and a spreadsheet are available from Chipcon generating configuration data for any frequency giving optimum sensitivity.

ISM Frequency [MHz]	Actual frequency [MHz]	Crystal frequency [MHz]	Low-side / high- side LO*	Reference divider REFDIV	Frequency word RX mode FREQ	Frequency word TX mode FREQ	Frequency seperation FSEP
315	315.037200	7.3728	High-side	7	4894720	4891888	995
		11.0592		10	4661248	4658551	948
433.3	433.302000	3.6864	Low-side	3	5767168	5768741	853
		7.3728		6	5767168	5768741	853
		11.0592		9	5767168	5768741	853
433.9	433.916400	3.6864	Low-side	3	5775360	5776933	853
		7.3728		6	5775360	5776933	853
		11.0592		9	5775360	5776933	853
434.5	434.530800	3.6864	Low-side	3	5783552	5785125	853
		7.3728		6	5783552	5785125	853
		11.0592		9	5783552	5785125	853
868.3	868.297200	3.6864	Low-side	2	7708672	7709720	568
		7.3728		4	7708672	7709720	568
		11.0592		5	6422528	6423402	474
868.95	868.918800	3.6864	High-side	2	7716864	7715246	568
		7.3728		4	7716864	7715246	568
		11.0592		6	7716864	7715246	568
869.525	869.526000	3.6864	Low-side	3	11583488	11585061	853
		7.3728		6	11583488	11585061	853
		11.0592		9	11583488	11585061	853
869.85	869.840400	3.6864	High-side	2	7725056	7723438	568
		7.3728		4	7725056	7723438	568
		11.0592		6	7725056	7723438	568
915	914.998800	3.6864	High-side	2	8126464	8124846	568
		7.3728		4	8126464	8124846	568
		11.0592		6	8126464	8124846	568

*Note: When using low-side LO injection the data at DIO will be inverted.

Table 8. Recommended settings for ISM frequencies

VCO

Only one external inductor (L101) is required for the VCO. The inductor will determine the operating frequency range of the circuit. It is important to place the inductor as close to the pins as possible in order to reduce stray inductance. It is recommended to use a high Q, low tolerance inductor for best performance.

Typical tuning range for the integrated varactor is 20-25%.

Component values for various frequencies are given in Table 1. Component values for other frequencies can be found using the SmartRF Studio software.

VCO and PLL self-calibration

To compensate for supply voltage, temperature and process variations the VCO and PLL must be calibrated. The calibration is done automatically and sets maximum VCO tuning range and optimum charge pump current for PLL stability. After setting up the device at the operating frequency, the self-calibration can be initiated by setting the *CAL_START* bit. The calibration result is stored internally in the chip, and is valid as long as power is not turned off. If large supply voltage variations (more than 0.5 V) or temperature variations (more than 40 degrees) occur after calibration, a new calibration should be performed.

The self-calibration is controlled through the *CAL* register (see configuration registers description p. 37). The *CAL_COMPLETE* bit indicates complete calibration. The user can poll this bit, or simply wait for 34 ms (calibration wait time when *CAL_WAIT* = 1). The wait time is proportional to the internal PLL reference frequency. The lowest permitted reference frequency (1 MHz) gives 34 ms wait time, which is therefore the worst case.

Reference frequency [MHz]	Calibration time [ms]
2.4	14
2.0	17
1.5	23
1.0	34

The *CAL_COMPLETE* bit can also be monitored at the CHP_OUT (LOCK) pin (configured by *LOCK_SELECT[3:0])* and used as an interrupt input to the microcontroller.

The CAL_START bit must be set to 0 by the microcontroller after the calibration is done.

There are separate calibration values for the two frequency registers. If the two frequencies, A and B, differ more than 1 MHz, or different VCO currents are used (*VCO_CURRENT[3:0]* in the *CURRENT* register) the calibration should be done separately. When using a 10.7 MHz external IF the LO is 10.7 MHz below/above the transmit frequency, hence separate calibration must be done. The *CAL_DUAL* bit in the *CAL* register controls dual or separate calibration.

The single calibration algorithm using separate calibration for RX and TX frequency is illustrated in Figure 14.

In Figure 15 the dual calibration algorithm is shown for two RX frequencies. It could also be used for two TX frequencies, or even for one RX and one TX frequency if the same VCO current is used.

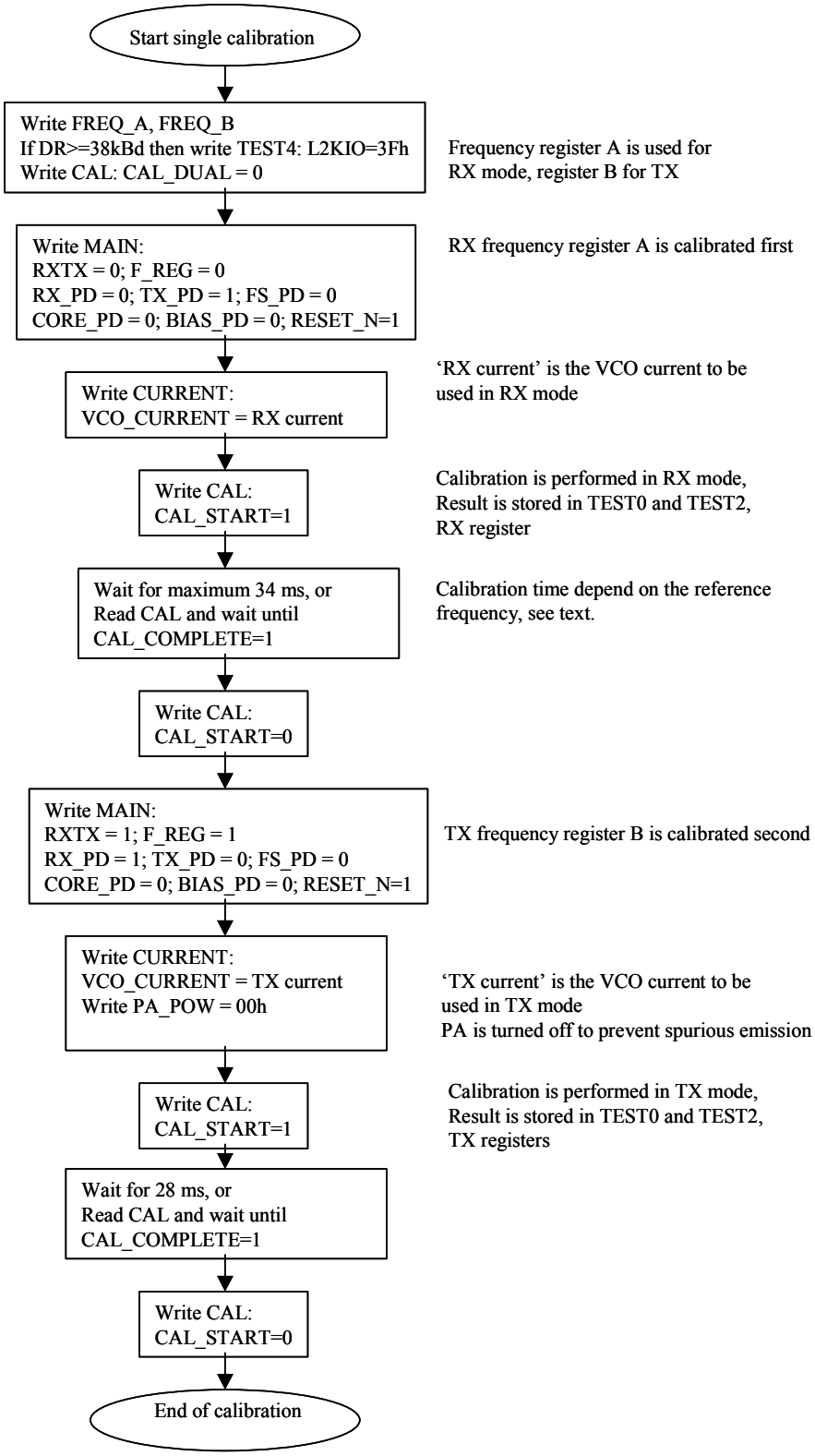


Figure 14. Single calibration algorithm for RX and TX

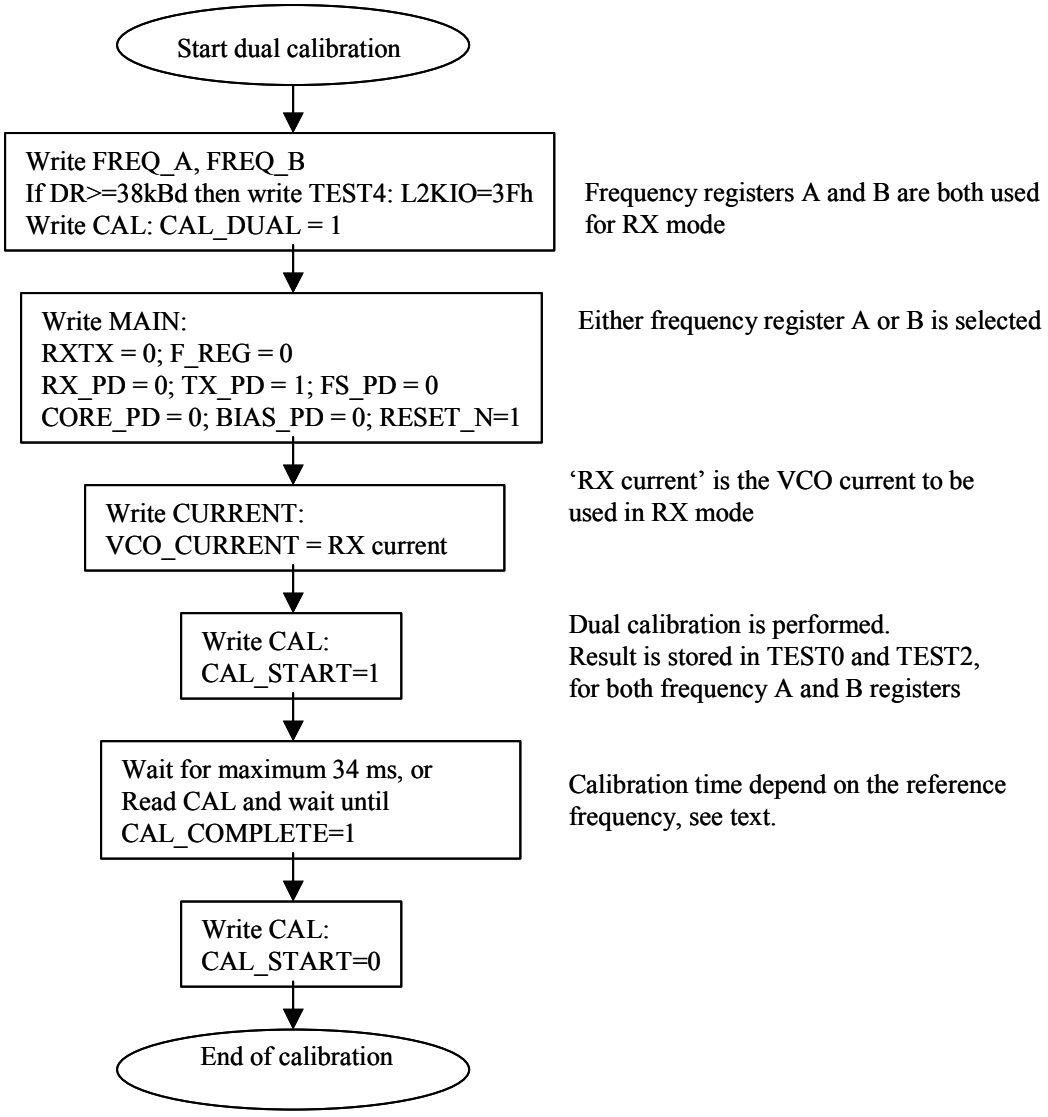


Figure 15. Dual calibration algorithm for RX mode

VCO and LNA current control

The VCO current is programmable and should be set according to operating frequency RX/TX mode and output power. Recommended settings for the *VCO_CURRENT* bits in the *CURRENT* register are shown in the tables on page 39.

The bias current for the LNA, and the LO and PA buffers are also programmable. Table 9 shows the current consumption and receiver sensitivity for different settings (2.4 kBaud Manchester encoded data).

RF freq-uency [MHz]	Current consumption [mA]	Sensitivity [dBm]	CURRENT register			FRONT_END register	
			VCO_ CURRENT [3:0]	LO_DRIVE [1:0]	PA_DRIVE [1:0]	BUF_CUR RENT	LNA_CUR RENT[1:0]
433	9.3	-110	0100	01	00	0	10
433	7.4	-109	0100	00	00	0	00
868	11.8	-107	1000	11	00	1	10
868	9.6	-105	1000	10	00	0	00

Note: Current consumption and sensitivity are typical figures at 2.4 kBaud Manchester encoded data, BER 10^{-3}

Table 9. Receiver sensitivity as function of current consumption

Power management

CC1000 offers great flexibility for power management in order to meet strict power consumption requirements in battery operated applications. Power Down mode is controlled through the *MAIN* register. There are separate bits to control the RX part, the TX part, the frequency synthesiser and the crystal oscillator (see page 37). This individual control can be used to optimise for lowest possible current consumption in a certain application.

A typical power-on and initialising sequence for minimum power consumption is shown in Figure 16 and Figure 17.

PALE should be tri-stated or set to a high level during power down mode in order to prevent a trickle current from flowing in the internal pull-up resistor.

PA_POW should be set to 00h before power down mode to ensure lowest possible leakage current.

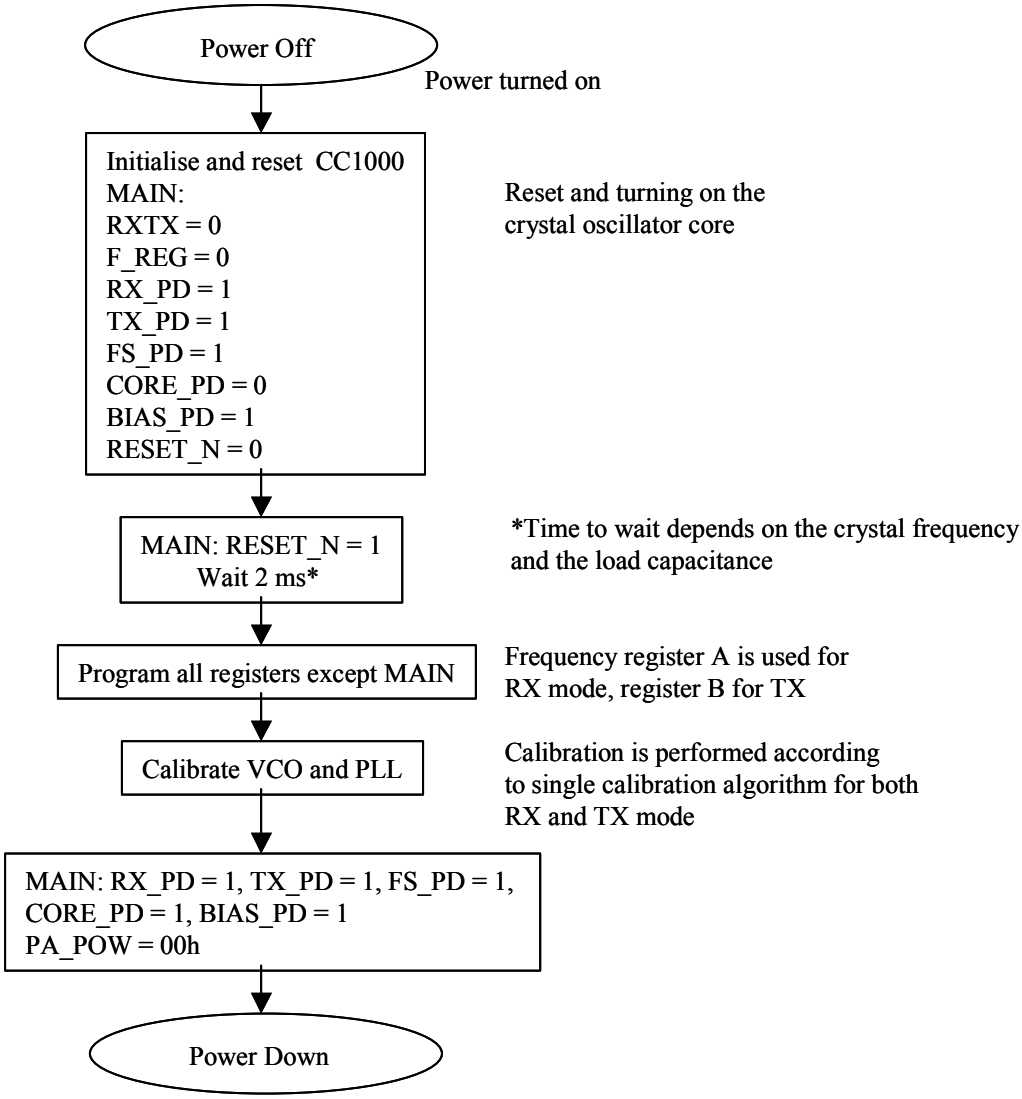


Figure 16. Initializing sequence

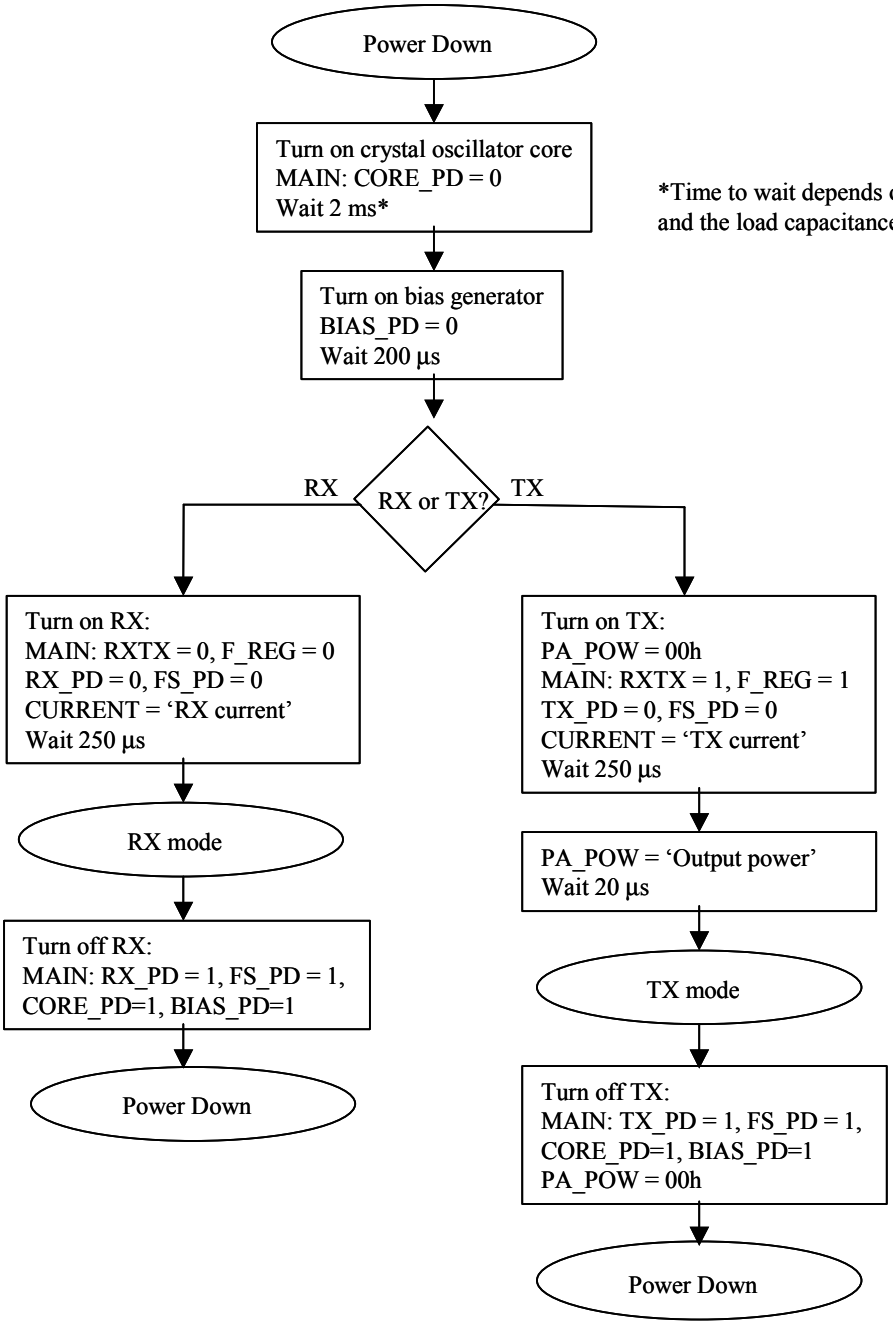


Figure 17. Sequence for activating RX or TX mode

Input / Output Matching

A few passive external components combined with the internal T/R switch circuitry ensures match in both RX and TX mode. The matching network is shown in Figure 18. Component values for various frequencies are given in Table 1. Component values for other frequencies can be found using the configuration software.

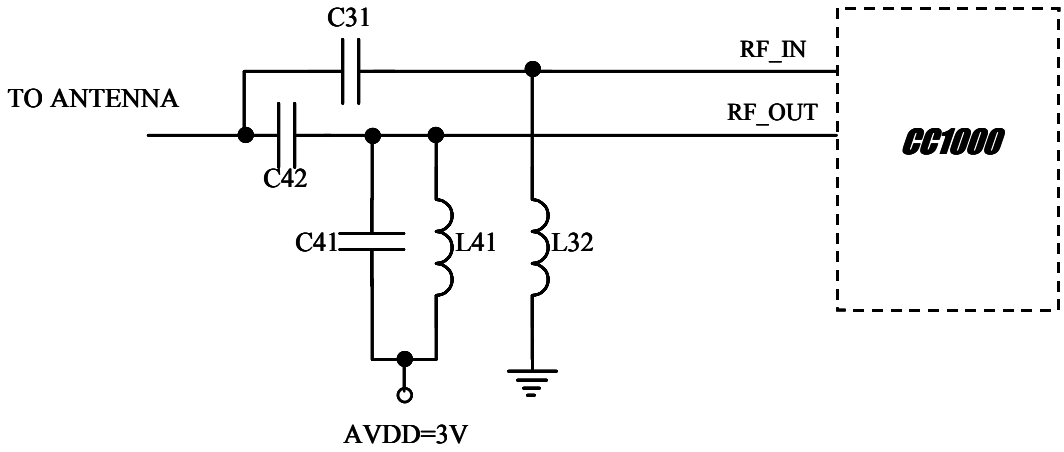


Figure 18. Input/output matching network

Output power programming

The RF output power is programmable and controlled by the PA_POW register. Table 10 shows the closest programmable value for output powers in steps of 1 dB. The typical current consumption is also shown.

In power down mode the PA_POW should be set to 00h for minimum leakage current.

Output power [dBm]	RF frequency 433 MHz		RF frequency 868 MHz	
	PA_POW [hex]	Current consumption, typ. [mA]	PA_POW [hex]	Current consumption, typ. [mA]
-20	01	5.3	02	8.6
-19	01	6.9	02	8.8
-18	02	7.1	03	9.0
-17	02	7.1	03	9.0
-16	02	7.1	04	9.1
-15	03	7.4	05	9.3
-14	03	7.4	05	9.3
-13	03	7.4	06	9.5
-12	04	7.6	07	9.7
-11	04	7.6	08	9.9
-10	05	7.9	09	10.1
-9	05	7.9	0B	10.4
-8	06	8.2	0C	10.6
-7	07	8.4	0D	10.8
-6	08	8.7	0F	11.1
-5	09	8.9	40	13.8
-4	0A	9.6	50	14.5
-3	0B	9.4	50	14.5
-2	0C	9.7	60	15.1
-1	0E	10.2	70	15.8
0	0F	10.4	80	16.8
1	40	11.8	90	17.2
2	50	12.8	B0	18.5
3	50	12.8	C0	19.2
4	60	13.8	F0	21.3
5	70	14.8	FF	25.4
6	80	15.8		
7	90	16.8		
8	C0	20.0		
9	E0	22.1		
10	FF	26.7		

Table 10. Output power settings and typical current consumption

RSSI output

CC1000 has a built-in RSSI (Received Signal Strength Indicator) giving an analogue output signal at the RSSI/IF pin. The *IF_RSSI* bits in the *FRONT_END* register enable the RSSI. When the RSSI function is enabled, the output current of this pin is inversely proportional to the input signal level. The output should be terminated in a resistor to convert the current output into a voltage. A capacitor is used in order to low-pass filter the signal.

The RSSI voltage range from 0 – 1.2 V when using a 27 kΩ terminating resistor, giving approximately 50 dB/V. This RSSI voltage can be measured by an A/D converter. Note that a higher voltage means a lower input signal.

The RSSI measures the power referred to the RF_IN pin. The input power can be calculated using the following equations:

$P = -51.3\ V_{RSSI} - 49.2$ [dBm] at 433 MHz
$P = -50.0\ V_{RSSI} - 45.5$ [dBm] at 868 MHz

The external network for RSSI operation is shown in Figure 19. R281 = 27 kΩ, C281 = 1nF.

A typical plot of RSSI voltage as function of input power is shown in Figure 20.

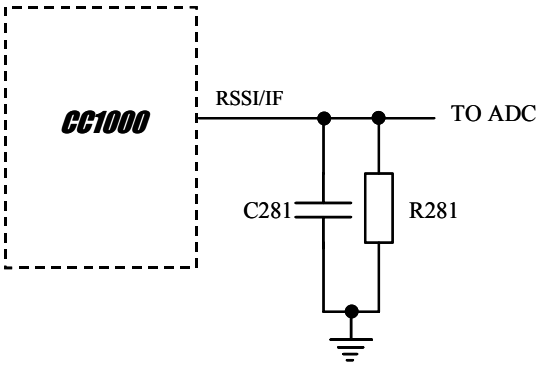


Figure 19. RSSI circuit

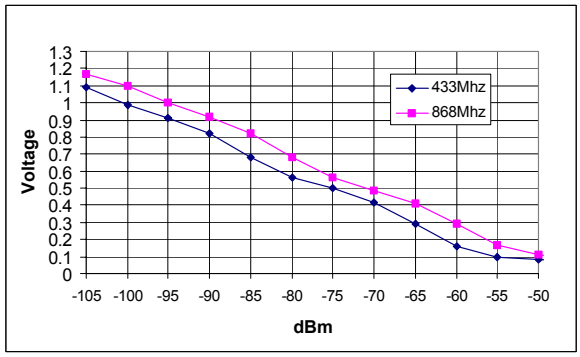


Figure 20. RSSI voltage vs. input power

IF output

CC1000 has a built-in 10.7 MHz IF output buffer. This buffer could be applied in narrow-band applications with requirements on mirror image filtering. The system is then built with ***CC1000***, a 10.7 MHz ceramic filter and an external 10.7 MHz demodulator. The external network for IF output operation is shown in Figure 21. R281 = 470 Ω, C281 = 3.3nF.

The external network provides 330 Ω source impedance for the 10.7 MHz ceramic filter.

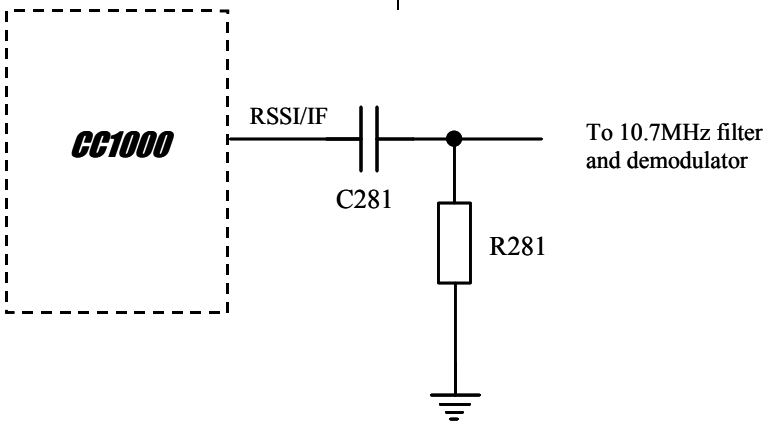


Figure 21. IF output circuit

Crystal oscillator

An external clock signal or the internal crystal oscillator can be used as main frequency reference. An external clock signal should be connected to XOSC_Q1, while XOSC_Q2 should be left open. The *XOSC_BYPASS* bit in the *FRONT_END* register should be set when an external clock signal is used.

The crystal frequency should be in the range 3-4, 6-8 or 9-16 MHz. Because the crystal frequency is used as reference for the data rate (as well as other internal functions), the following frequencies are recommended: 3.6864, 7.3728, 11.0592 or 14.7456 MHz. These frequencies will give accurate data rates. The crystal frequency range is selected by *XOSC_FREQ1:0* in the *MODEM0* register.

To operate in synchronous mode at data rates different from the standards at 1.2, 2.4, 4.8 kBaud and so on, the crystal frequency can be scaled. The data rate (DR) will change proportionally to the new crystal frequency (f). To calculate the new crystal frequency:

$$f_{xtal\_new} = f_{xtal} \frac{DR_{new}}{DR}$$

Using the internal crystal oscillator, the crystal must be connected between XOSC_Q1 and XOSC_Q2. The oscillator is designed for parallel mode operation of the crystal. In addition loading capacitors (C171 and C181) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{171}} + \frac{1}{C_{181}}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Typically the total parasitic capacitance is 8 pF. A trimming capacitor may be placed across C171 for initial tuning if necessary.

The crystal oscillator circuit is shown in Figure 22. Typical component values for different values of C_L are given in Table 11.

The initial tolerance, temperature drift, ageing and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application. By specifying the *total* expected frequency accuracy in SmartRF Studio together with data rate and frequency separation, the software will calculate the total bandwidth and compare to the available IF bandwidth. Any contradictions will be reported by the software and a more accurate crystal will be recommended if required.

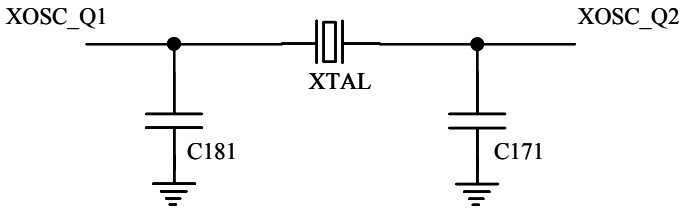


Figure 22. Crystal oscillator circuit

Item	C_L= 12 pF	C_L= 16 pF	C_L= 22 pF
C171	6.8 pF	18 pF	33 pF
C181	6.8 pF	18 pF	33 pF

Table 11. Crystal oscillator component values

Frequency spectrum shaping and dithering

The ***CC1000*** has the unique possibility of frequency spectrum shaping and dithering. The inherent abrupt frequency change using FSK modulation gives a broad RF spectrum. By using a smooth frequency shift, the spectrum broadening can be reduced, see Figure 23. This smooth frequency shift can be implemented by stepping through several intermediate frequencies between the two FSK frequencies. ***CC1000*** use 16 intermediate frequencies that are specified in the seven *FSHAPE* registers. The frequency steps are made anti-symmetrical, hence only seven values are specified to define the 16 steps, see Figure 24. The data shaping is turned on using the *SHAPE* bit in the *FSCTRL* register.

The maximum frequency separation using frequency shaping is FSEP = 63.

The time-step is programmed in the *FSDELAY* register. This value should correspond to the data rate used. For equal spacing of steps through one baud period, use

$$FSDELAY = \frac{f_{ref}}{16 \cdot BaudRate} - 1$$

where the reference frequency, f_{ref}, is the crystal oscillator clock divided by *REFDIV*. Shorter time-steps could also be used.

The default values after reset correspond to a raised cosine frequency change for maximum deviation.

Dithering of the PLL can be used to reduce spurious signals originating from internal reference frequencies. The dithering is turned on by the *DITHER1* and *DITHER0* bits in the *FSCTRL* register.

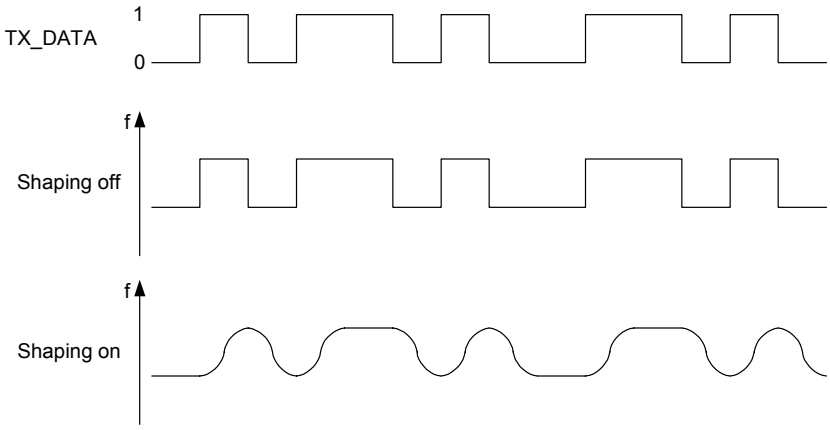


Figure 23. FSK spectrum shaping by smooth frequency transitions

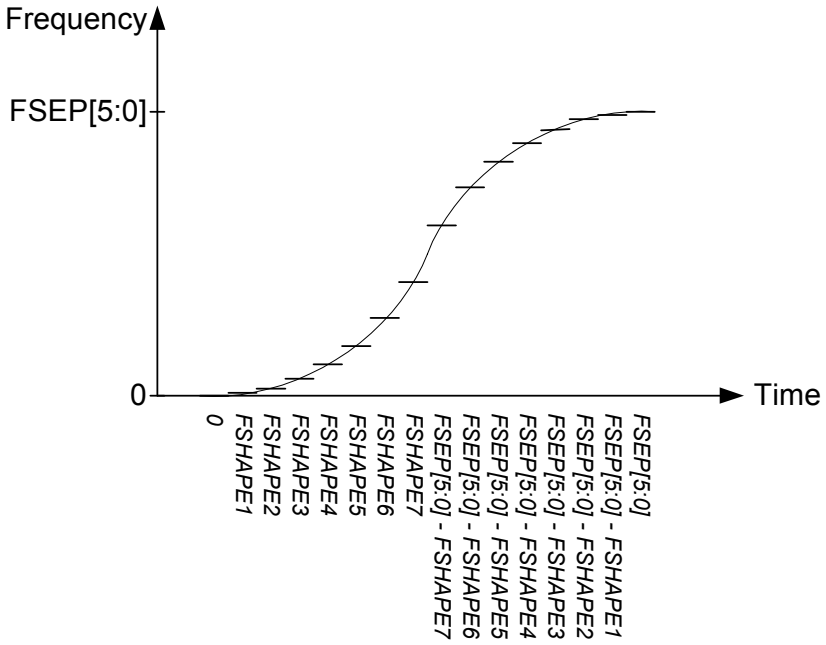


Figure 24. Stepwise frequency shaping

Optional LC Filter

An optional LC filter may be added between the antenna and the matching network in certain applications. The filter will reduce the emission of harmonics and increase the receiver selectivity.

The filter topology is shown in Figure 25. Component values are given in Table 12. The filter is designed for 50 Ω terminations. The component values may have to be tuned to compensate for layout parasitics.

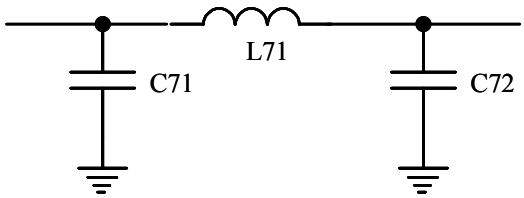


Figure 25. LC filter

Item	315 MHz	433 MHz	868 MHz	915 MHz
C71	30 pF	20 pF	10 pF	10 pF
C72	30 pF	20 pF	10 pF	10 pF
L71	15 nH	12 nH	5.6 nH	4.7 nH

Table 12. LC filter component values

System Considerations and Guidelines

SRD regulations
International regulations and national laws regulate the use of radio receivers and transmitters. SRDs (Short Range Devices) for licence free operation are allowed to operate in the 433 and 868-870 MHz bands in most European countries. In the United States such devices operate in the 260–470 and 902-928 MHz bands. ***CC1000*** is designed to meet the requirements for operation in all these bands. A summary of the most important aspects of these regulations can be found in Application Note *AN001 SRD regulations for licence free transceiver operation*, available from Chipcon's web site.

Low cost systems
In systems where low cost is of great importance the ***CC1000*** is the ideal choice. Very few external components keep the total cost at a minimum. The oscillator crystal can then be a low cost crystal with 50 ppm frequency tolerance.

Battery operated systems
In low power applications the power down mode should be used when not being active. Depending on the start-up time requirement, the oscillator core can be powered during power down. See page 25 for information on how effective power management can be implemented.

Narrow band systems
CC400 and CC900 are recommended for best performance in narrow band applications. The phase noise of CC400 / CC900 is superior and for systems with 25 kHz channel spacing with strict requirements to ACP (Adjacent Channel Power) low phase noise is important. If ***CC1000*** is used in a narrow band receiver, an external ceramic filter and demodulator is recommended.

A unique feature in ***CC1000*** is the very fine frequency resolution of 250 Hz. This can be used to do the temperature compensation of the crystal if the temperature drift curve is known and a temperature sensor is included in the system. Even initial adjustment can be done using the frequency programmability. This eliminates the need for an expensive TCXO and trimming in some applications. In less demanding applications a crystal with low temperature drift and low ageing could be used without further compensation. A trimmer capacitor in the crystal oscillator circuit (in parallel with C171) could be used to set the initial frequency accurately. The fine frequency step programming cannot be used in RX mode if optimised frequency settings are required (see page 21).

CC1000 also exhibits a unique spectrum-shaping feature in order to improve the ACP even for large data rates when using low deviation. In 'true' FSK systems with abrupt frequency shifting the spectrum is inherently broad. By making the frequency shift 'softer' the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth.

High reliability systems
Using a SAW filter as a preselector will improve the communication reliability in harsh environments by reducing the probability of blocking. The receiver sensitivity and the output power will be reduced due to the filter insertion loss. By inserting the filter in the RX path only, together with an external RX/TX switch, only the receiver sensitivity is reduced, and output power is remained. The CHP_OUT (LOCK) pin can be configured to control an external LNA, RX/TX switch or power amplifier. This is controlled by *LOCK_SELECT* in the *LOCK* register.

Frequency hopping spread spectrum systems
Due to the very fast frequency shift properties of the PLL, the ***CC1000*** is also suitable for frequency hopping systems. Hop rates of 1-100 hops/s are usually used depending on the bit rate and the amount of data to be sent during each transmission. The two frequency registers (*FREQ_A* and *FREQ_B*) are designed such that the 'next' frequency can be programmed while the 'present' frequency is used. The switching between the two frequencies is done through the *MAIN* register.

PCB Layout Recommendations

Chipcon provide reference layouts that should be followed in order to achieve the best performance. The CC1000PP Plug & Play reference design can be downloaded from the Chipcon website.

A two layer PCB is highly recommended. The bottom layer of the PCB should be the "ground-layer".

The top layer should be used for signal routing, and the open areas should be filled with metallisation connected to ground using several vias.

The ground pins should be connected to ground as close as possible to the package pin using individual vias. The de-coupling capacitors should also be placed as close as possible to the supply pins and connected to the ground plane by separate vias.

The external components should be as small as possible and surface mount devices are required. The VCO inductor must be placed as close as possible to the chip and symmetrical with respect to the input pins.

Precaution should be used when placing the microcontroller in order to avoid interference with the RF circuitry.

In certain applications where the ground plane for the digital circuitry is expected to be noisy, the ground plane may be split in an analogue and a digital part. All AGND pins and AVDD de-coupling capacitors should be connected to the analogue ground plane. All DGND pins and DVDD de-coupling capacitors should be connected to the digital ground. The connection between the two ground planes should be implemented as a star connection with the power supply ground.

A development kit with a fully assembled PCB is available, and can be used as a guideline for layout.

Antenna Considerations

CC1000 can be used together with various types of antennas. The most common antennas for short range communication are monopole, helical and loop antennas.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength (λ/4). They are very easy to design and can be implemented simply as a "piece of wire" or even integrated into the PCB.

Non-resonant monopole antennas shorter than λ/4 can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated into the PCB.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. But helical antennas tend to be more difficult to optimise than the simple monopole.

Loop antennas are easy to integrate into the PCB, but are less effective due to difficult impedance matching because of their very low radiation resistance.

For low power applications the λ/4-monopole antenna is recommended giving the best range and because of its simplicity.

The length of the λ/4-monopole antenna is given by:

$$L = 7125 / f$$

where f is in MHz, giving the length in cm. An antenna for 869 MHz should be 8.2 cm, and 16.4 cm for 434 MHz.

The antenna should be connected as close as possible to the IC. If the antenna is located away from the input pin the antenna should be matched to the feeding transmission line (50 Ω).

For a more thorough primer on antennas, please refer to Application *Note AN003 SRD Antennas* available from Chipcon's web site.

Configuration registers

The configuration of ***CC1000*** is done by programming the 29 8-bit configuration registers. The configuration data based on selected system parameters are most easily found by using the SmartRF Studio software. A complete description of the registers are given in the following tables. After a RESET is programmed all the registers have default values. The TEST registers are also set to default values after a RESET, and should not be altered by the user.

REGISTER OVERVIEW

ADDRESS	Byte Name	Description
00h	MAIN	MAIN Register
01h	FREQ_2A	Frequency Register 2A
02h	FREQ_1A	Frequency Register 1A
03h	FREQ_0A	Frequency Register 0A
04h	FREQ_2B	Frequency Register 2B
05h	FREQ_1B	Frequency Register 1B
06h	FREQ_0B	Frequency Register 0B
07h	FSEP1	Frequency Separation Register 1
08h	FSEP0	Frequency Separation Register 0
09h	CURRENT	Current Consumption Control Register
0Ah	FRONT_END	Front End Control Register
0Bh	PA_POW	PA Output Power Control Register
0Ch	PLL	PLL Control Register
0Dh	LOCK	LOCK Status Register and signal select to CHP_OUT (LOCK) pin
0Eh	CAL	VCO Calibration Control and Status Register
0Fh	MODEM2	Modem Control Register 2
10h	MODEM1	Modem Control Register 1
11h	MODEM0	Modem Control Register 0
12h	MATCH	Match Capacitor Array Control Register for RX and TX impedance matching
13h	FSCTRL	Frequency Synthesiser Control Register
14h	FSHAPE7	Frequency Shaping Register 7
15h	FSHAPE6	Frequency Shaping Register 6
16h	FSHAPE5	Frequency Shaping Register 5
17h	FSHAPE4	Frequency Shaping Register 4
18h	FSHAPE3	Frequency Shaping Register 3
19h	FSHAPE2	Frequency Shaping Register 2
1Ah	FSHAPE1	Frequency Shaping Register 1
1Bh	FSDELAY	Frequency Shaping Delay Register
1Ch	PRESCALER	Prescaler and IF-strip test control register
40h	TEST6	Test register for PLL LOOP
41h	TEST5	Test register for PLL LOOP
42h	TEST4	Test register for PLL LOOP
43h	TEST3	Test register for VCO
44h	TEST2	Test register for Calibration
45h	TEST1	Test register for Calibration
46h	TEST0	Test register for Calibration

MAIN Register (00h)

REGISTER	NAME	Default value	Active	Description
MAIN[7]	RXTX	-	-	RX/TX switch, 0 : RX , 1 : TX
MAIN[6]	F_REG	-	-	Selection of Frequency Register, 0 : Register A, 1 : Register B
MAIN[5]	RX_PD	-	H	Power Down of LNA, Mixer, IF, Demodulator, RX part of Signal Interface
MAIN[4]	TX_PD	-	H	Power Down of TX part of Signal Interface, PA
MAIN[3]	FS_PD	-	H	Power Down of Frequency Synthesiser
MAIN[2]	CORE_PD	-	H	Power Down of Crystal Oscillator Core
MAIN[1]	BIAS_PD	-	H	Power Down of BIAS (Global_Current_Generator) and Crystal Oscillator Buffer
MAIN[0]	RESET_N	-	L	Reset, active low. Writing RESET_N low will write default values to all other registers than MAIN. Bits in MAIN do not have a default value, and will be written directly through the configurations interface. Must be set high to complete reset.

FREQ_2A Register (01h)

REGISTER	NAME	Default value	Active	Description
FREQ_2A[7:0]	FREQ_A[23:16]	01110101	-	8 MSB of frequency control word A

FREQ_1A Register (02h)

REGISTER	NAME	Default value	Active	Description
FREQ_1A[7:0]	FREQ_A[15:8]	10100000	-	Bit 15 to 8 of frequency control word A

FREQ_0A Register (03h)

REGISTER	NAME	Default value	Active	Description
FREQ_0A[7:0]	FREQ_A[7:0]	11001011	-	8 LSB of frequency control word A

FREQ_2B Register (04h)

REGISTER	NAME	Default value	Active	Description
FREQ_2B[7:0]	FREQ_B[23:16]	01110101	-	8 MSB of frequency control word B

FREQ_1B Register (05h)

REGISTER	NAME	Default value	Active	Description
FREQ_1B[7:0]	FREQ_B[15:8]	10100101	-	Bit 15 to 8 of frequency control word B

FREQ_0B Register (06h)

REGISTER	NAME	Default value	Active	Description
FREQ_0B[7:0]	FREQ_B[7:0]	01001110	-	8 LSB of frequency control word B

FSEP1 Register (07h)

REGISTER	NAME	Default value	Active	Description
FSEP1[7:3]	-	-	-	Not used
FSEP1[2:0]	FSEP_MSB[2:0]	000	-	3 MSB of frequency separation control

FSEP0 Register (08h)

REGISTER	NAME	Default value	Active	Description
FSEP0[7:0]	FSEP_LSB[7:0]	01011001	-	8 LSB of frequency separation control

CURRENT Register (09h)

REGISTER	NAME	Default value	Active	Description
CURRENT[7:4]	VCO_CURRENT[3:0]	1100	-	Control of current in VCO core for TX and RX 0000 : 150µA 0001 : 250µA 0010 : 350µA 0011 : 450µA 0100 : 950µA, use for RX, f= 400 - 500 MHz 0101 : 1050µA 0110 : 1150µA 0111 : 1250µA 1000 : 1450µA, use for RX, f<400 MHz and f>500 MHz; and TX, f= 400 - 500 MHz 1001 : 1550µA, use for TX, f<400 MHz 1010 : 1650µA 1011 : 1750µA 1100 : 2250µA 1101 : 2350µA 1110 : 2450µA 1111 : 2550µA, use for TX, f>500 MHz
CURRENT[3:2]	LO_DRIVE[1:0]	10		Control of current in VCO buffer for LO drive 00 : 0.5mA, use for TX 01 : 1.0mA , use for RX, f<500 MHz 10 : 1.5mA, 11 : 2.0mA, use for RX, f>500 MHz
CURRENT[1:0]	PA_DRIVE[1:0]	10		Control of current in VCO buffer for PA 00 : 1mA, use for RX 01 : 2mA, use for TX, f<500 MHz 10 : 3mA 11 : 4mA, use for TX, f>500 MHz

FRONT_END Register (0Ah)

REGISTER	NAME	Default value	Active	Description
FRONT_END[7:6]	-	00	-	Not used
FRONT_END[5]	BUF_CURRENT	0	-	Control of current in the LNA_FOLLOWER 0 : 520uA, use for f<500 MHz 1 : 690uA, use for f>500 MHz
FRONT_END[4:3]	LNA_CURRENT [1:0]	01	-	Control of current in LNA 00 : 0.8mA, use for f<500 MHz 01 : 1.4mA 10 : 1.8mA, use for f>500 MHz 11 : 2.2mA
FRONT_END[2:1]	IF_RSSI[1:0]	00	-	Control of IF_RSSI pin 00 : Internal IF and demodulator, RSSI inactive 01 : RSSI active, RSSI/IF is analog RSSI output 10 : External IF and demodulator, RSSI/IF is mixer output. Internal IF in power down mode. 11 : Not used
FRONT_END[0]	XOSC_BYPASS	0	-	0 : Internal XOSC enabled 1 : Power-Down of XOSC, external CLK used

PA_POW Register (0Bh)

REGISTER	NAME	Default value	Active	Description
PA_POW[7:4]	PA_HIGHPOWER[3:0]	0000	-	Control of output power in high power array. Should be 0000 in PD mode . See Table 10 page 29 for details.
PA_POW[3:0]	PA_LOWPOWER[3:0]	1111	-	Control of output power in low power array Should be 0000 in PD mode. See Table 10 page 29 for details.

PLL Register (0Ch)

REGISTER	NAME	Default value	Active	Description
PLL[7]	EXT_FILTER	0	-	1 : External loop filter 0 : Internal loop filter 1-to-0 transition samples F_COMP comparator when BREAK_LOOP=1 (TEST3)
PLL[6:3]	REFDIV[3:0]	0010	-	Reference divider 0000 : Not allowed 0001 : Not allowed 0010 : Divide by 2 0011 : Divide by 3 ..... 1111 : Divide by 15
PLL[2]	ALARM_DISABLE	0	h	0 : Alarm function enabled 1 : Alarm function disabled
PLL[1]	ALARM_H	-	-	Status bit for tuning voltage out of range (too close to VDD)
PLL[0]	ALARM_L	-	-	Status bit for tuning voltage out of range (too close to GND)

LOCK Register (0Dh)

REGISTER	NAME	Default value	Active	Description
LOCK[7:4]	LOCK_SELECT[3:0]	0000	-	Selection of signals to CHP_OUT (LOCK) pin 0000 : Normal, pin can be used as CHP_OUT 0001 : LOCK_CONTINUOUS (active high) 0010 : LOCK_INSTANT (active high) 0011 : ALARM_H (active high) 0100 : ALARM_L (active high) 0101 : CAL_COMPLETE (active high) 0110 : IF_OUT 0111 : REFERENCE_DIVIDER Output 1000 : TX_PDB (active high, activates external PA when TX_PD=0) 1001 : Manchester Violation (active high) 1010 : RX_PDB (active high, activates external LNA when RX_PD=0) 1011 : Not defined 1100 : Not defined 1101 : LOCK_AVG_FILTER 1110 : N_DIVIDER Output 1111 : F_COMP
LOCK[3]	PLL_LOCK_ ACCURACY	0	-	0 : Sets Lock Threshold = 127, Reset Lock Threshold = 111. Corresponds to a worst case accuracy of 0.7% 1 : Sets Lock Threshold = 31, Reset Lock Threshold =15. Corresponds to a worst case accuracy of 2.8%
LOCK[2]	PLL_LOCK_ LENGTH	0	-	0 : Normal PLL lock window 1 : Not used
LOCK[1]	LOCK_INSTANT	-	-	Status bit from Lock Detector
LOCK[0]	LOCK_CONTINUOUS	-	-	Status bit from Lock Detector

CAL Register (0Eh)

REGISTER	NAME	Default value	Active	Description
CAL[7]	CAL_START	0	↑	↑ 1 : Calibration started 0 : Calibration inactive CAL_START must be set to 0 after calibration is done
CAL[6]	CAL_DUAL	0	H	1 : Store calibration in both A and B 0 : Store calibration in A or B defined by MAIN[6]
CAL[5]	CAL_WAIT	0	H	1 : Normal Calibration Wait Time 0 : Half Calibration Wait Time The calibration time is proportional to the internal reference frequency. 2 MHz reference frequency gives 14 ms wait time.
CAL[4]	CAL_CURRENT	0	H	1 : Calibration Current Doubled 0 : Normal Calibration Current
CAL[3]	CAL_COMPLETE	0	H	Status bit defining that calibration is complete
CAL[2:0]	CAL_ITERATE	101	H	Iteration start value for calibration DAC 000 - 101: Not used 110 : Normal start value 111 : Not used

MODEM2 Register (0Fh)

REGISTER	NAME	Default value	Active	Description
MODEM2[7]	PEAKDETECT	1	H	Peak Detector and Remover disabled or enabled 0 : Peak detector and remover is disabled 1 : Peak detector and remover is enabled
MODEM2[6:0]	PEAK_LEVEL_OFFSET[6:0]	0010110	-	Threshold level for Peak Remover in Demodulator. Correlated to frequency deviation, see note.

Note: PEAK_LEVEL_OFFSET[6:0] = $\frac{Fs}{IF_{low}} - \frac{Fs}{IF_{low} + \Delta f/2} \cdot \frac{5}{8}$ where $Fs = \frac{f\_xosc}{XOSC\_FREQ + 1}$

and $IF_{low} = 150kHz - 2 \bullet f\_rf \bullet XTAL\_accuracy$ and Δf is the separation

MODEM1 Register (10h)

REGISTER	NAME	Default value	Active	Description
MODEM1[7:5]	MLIMIT	011	-	Sets the limit for the Manchester Violation Flag. A Manchester Value = 14 is a perfect bit and a Manchester Value = 0 is a constant level (an unbalanced corrupted bit) 000 : No Violation Flag is set 001 : Violation Flag is set for Manchester Value < 1 010 : Violation Flag is set for Manchester Value < 2 011 : Violation Flag is set for Manchester Value < 3 100 : Violation Flag is set for Manchester Value < 4 101 : Violation Flag is set for Manchester Value < 5 110 : Violation Flag is set for Manchester Value < 6 111 : Violation Flag is set for Manchester Value < 7
MODEM1[4]	LOCK_AVG_IN	0	H	Lock control bit of Average Filter 0 : Average Filter is free-running 1 : Average Filter is locked
MODEM1[3]	LOCK_AVG_MODE	0	-	Automatic lock of Average Filter 0 : Lock of Average Filter is controlled automatically 1 : Lock of Average Filter is controlled by LOCK_AVG_IN
MODEM1[2:1]	SETTLING[1:0]	11	-	Settling Time of Average Filter 00 : 11 baud settling time, worst case 1.2dB loss in sensitivity 01 : 22 baud settling time, worst case 0.6dB loss in sensitivity 10 : 43 baud settling time, worst case 0.3dB loss in sensitivity 11 : 86 baud settling time, worst case 0.15dB loss in sensitivity
MODEM1[0]	MODEM_RESET_N	1	L	Separate reset of MODEM

MODEM0 Register (11h)

REGISTER	NAME	Default value	Active	Description
MODEM0[7]	-	-	-	Not used
MODEM0[6:4]	BAUDRATE[2:0]	010	-	000 : 0.6 kBaud 001 : 1.2 kBaud 010 : 2.4 kBaud 011 : 4.8 kBaud 100 : 9.6 kBaud 101 : 19.2, 38.4 and 76.8 kBaud 110 : Not used 111 : Not used
MODEM0[3:2]	DATA_FORMAT[1:0]	01	-	00 : NRZ operation. 01 : Manchester operation 10 : Transparent Asyncronous UART operation 11 : Not used
MODEM0[1:0]	XOSC_FREQ[1:0]	00	-	Selection of XTAL frequency range 00 : 3MHz - 4MHz crystal, 3.6864MHz recommended Also used for 76.8 kBaud, 14.7456MHz 01 : 6MHz - 8MHz crystal, 7.3728MHz recommended Also used for 38.4 kBaud, 14.7456MHz 10 : 9MHz - 12MHz crystal, 11.0592 MHz recommended 11 : 12MHz - 16MHz crystal, 14.7456MHz recommended

MATCH Register (12h)

REGISTER	NAME	Default value	Active	Description
MATCH[7:4]	RX_MATCH[3:0]	0000	-	Selects matching capacitor array value for RX, step size is 0.4 pF 0010: Use for RF frequency > 500 MHz 0111: Use for RF frequency < 500 MHz
MATCH[3:0]	TX_MATCH[3:0]	0000	-	Selects matching capacitor array value for TX, step size is 0.4 pF

FSCTRL Register (13h)

REGISTER	NAME	Default value	Active	Description
FSCTRL[7:4]	-	-	-	Not used
FSCTRL[3]	DITHER1	0	H	Enable dithering when transmitting '1'
FSCTRL[2]	DITHER0	0	H	Enable dithering during RX, and when transmitting '0'
FSCTRL[1]	SHAPE	0	H	Enable data shaping
FSCTRL[0]	FS_RESET_N	1	L	Separate reset of shaping sequencer

FSHAPE7 Register (14h)

REGISTER	NAME	Default value	Active	Description
FSHAPE7[7:5]	--	-	-	Not used
FSHAPE7[4:0]	FSHAPE7	00001	-	Frequency shape register 1, used when *SHAPE* in *FSCTRL* is active.

FSHAPE6 Register (15h)

REGISTER	NAME	Default value	Active	Description
FSHAPE6[7:5]	-	-	-	Not used
FSHAPE6[4:0]	FSHAPE6	00011	-	Frequency shape register 2, used when *SHAPE* in *FSCTRL* is active.

FSHAPE5 Register (16h)

REGISTER	NAME	Default value	Active	Description
FSHAPE5[7:5]	-	-	-	Not used
FSHAPE5[4:0]	FSHAPE5	00110	-	Frequency shape register 3, used when *SHAPE* in *FSCTRL* is active.

FSHAPE4 Register (17h)

REGISTER	NAME	Default value	Active	Description
FSHAPE4[7:5]	-	-	-	Not used
FSHAPE4[4:0]	FSHAPE4	01010	-	Frequency shape register 4, used when *SHAPE* in *FSCTRL* is active.

FSHAPE3 Register (18h)

REGISTER	NAME	Default value	Active	Description
FSHAPE3[7:5]	-	-	-	Not used
FSHAPE3[4:0]	FSHAPE3	10000	-	Frequency shape register 5, used when *SHAPE* in *FSCTRL* is active.

FSHAPE2 Register (19h)

REGISTER	NAME	Default value	Active	Description
FSHAPE2[7:5]	-	-	-	Not used
FSHAPE2[4:0]	FSHAPE2	10110	-	Frequency shape register 6, used when *SHAPE* in *FSCTRL* is active.

FSHAPE1 Register (1Ah)

REGISTER	NAME	Default value	Active	Description
FSHAPE1[7:5]	-	-	-	Not used
FSHAPE1[4:0]	FSHAPE1	11100	-	Frequency shape register 7, used when *SHAPE* in *FSCTRL* is active.

FSDELAY Register (1Bh)

REGISTER	NAME	Default value	Active	Description
FSDELAY[7:0]	FSDELAY[7:0]	00101111	-	Sets the number of clock cycles delay between the use of the FSHAPE registers during frequency shaping

PRESCALER Register (1Ch)

REGISTER	NAME	Default value	Active	Description
PRESCALER[7:6]	PRE_SWING[1:0]	00	-	Prescaler swing. Fractions for PRE_CURRENT[1:0] = 00 00 : 1 * Nominal Swing 01 : 2/3 * Nominal Swing 10 : 7/3 * Nominal Swing 11 : 5/3 * Nominal Swing
PRESCALER[5:4]	PRE_CURRENT [1:0]	00	-	Prescaler current scaling 00 : 1 * Nominal Current 01 : 2/3 * Nominal Current 10 : 1/2 * Nominal Current 11 : 2/5 * Nominal Current
PRESCALER[3]	IF_INPUT	0	-	0 : Nominal setting 1 : RSSI/IF pin is input to IF-strips
PRESCALER[2]	IF_FRONT	0	-	0 : Nominal setting 1 : Output of IF_Front_amp is switched to RSSI/IF pin
PRESCALER[1:0]	-	00	-	Not used

TEST6 Register (for test only, 40h)

REGISTER	NAME	Default value	Active	Description
TEST6[7]	LOOPFILTER_TP1	0	-	1 : Select testpoint 1 to CHP_OUT 0 : CHP_OUT tied to GND
TEST6 [6]	LOOPFILTER_TP2	0	-	1 : Select testpoint 2 to CHP_OUT 0 : CHP_OUT tied to GND
TEST6 [5]	CHP_OVERRIDE	0	-	1 : use CHP_CO[4:0] value 0 : use calibrated value
TEST6[4:0]	CHP_CO[4:0]	10000	-	Charge_Pump Current DAC override value

TEST5 Register (for test only, 41h)

REGISTER	NAME	Default value	Active	Description
TEST5[7:6]	-	-	-	Not used
TEST5[5]	CHP_DISABLE	0	-	1 : CHP up and down pulses disabled 0 : normal operation
TEST5[4]	VCO_OVERRIDE	0	-	1 : use VCO_AO[2:0] value 0 : use calibrated value
TEST5[3:0]	VCO_AO[3:0]	1000	-	VCO_ARRAY override value

TEST4 Register (for test only, 42h)

REGISTER	NAME	Default value	Active	Description
TEST4[7:6]	-	-	-	Not used
TEST4[5:0]	L2KIO[5:0]	100101	h	Constant setting charge pump current scaling/rounding factor. Sets Bandwidth of PLL. Use 3Fh for 38.4 and 76.8 kBaud

TEST3 Register (for test only, 43h)

REGISTER	NAME	Default value	Active	Description
TEST3[7:5]	-	-	-	Not used
TEST3[4]	BREAK_LOOP	0	-	1 : PLL loop open 0 : PLL loop closed
TEST3[3:0]	CAL_DAC_OPEN	0100	-	Calibration DAC override value, active when BREAK_LOOP =1

TEST2 Register (for test only, 44h)

REGISTER	NAME	Default value	Active	Description
TEST2[7:5]	-	-	-	Not used
TEST2[4:0]	CHP_CURRENT [4:0]	-	-	Status vector defining applied CHP_CURRENT value

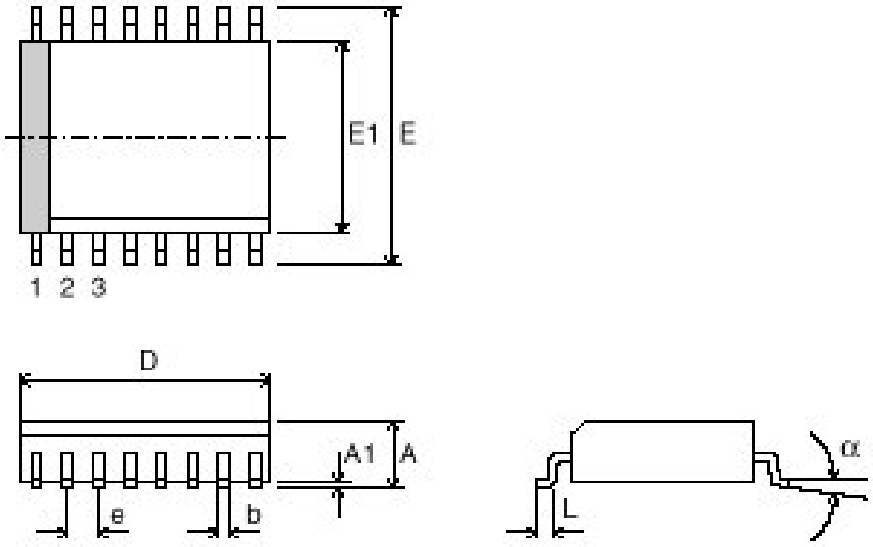
TEST1 Register (for test only, 45h)

REGISTER	NAME	Default value	Active	Description
TEST1[7:4]	-	-	-	Not used
TEST1[3:0]	CAL_DAC[3:0]	-	-	Status vector defining applied Calibration DAC value

TEST0 Register (for test only, 46h)

REGISTER	NAME	Default value	Active	Description
TEST0[7:4]	-	-	-	Not used
TEST0[3:0]	VCO_ARRAY[3:0]	-	-	Status vector defining applied VCO_ARRAY value

Package Description (TSSOP-28)



Note: The figure is an illustration only.

Thin Shrink Small Outline Package (TSSOP)											
		D	E1	E	A	A1	e	B	L	Copl.	α
TSSOP 28	Min	9.60	4.30	6.40		0.05	0.65	0.19	0.45		0°
	Max	9.80	4.50		1.20	0.15		0.30	0.75	0.10	8°
All dimensions in mm											

Soldering Information

Recommended soldering profile is according to CECC 00 802, Edition 3

Plastic Tube Specification

TSSOP 4.4mm (.173") antistatic tube.

Tube Specification				
Package	Tube Width	Tube Height	Tube Length	Units per Tube
TSSOP 28	268 mil	80 mil	20"	50

Carrier Tape and Reel Specification

Carrier tape and reel is in accordance with EIA Specification 481.

Tape and Reel Specification					
Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
TSSOP 28	16 mm	8 mm	4 mm	13"	2500

Ordering Information

Ordering part number	Description	MOQ
CC1000	Single Chip RF Transceiver	50 (tube)
CC1000/T&R	Single Chip RF Transceiver	2500 (tape and reel)
CC1000DK-433	CC1000 Development Kit, 433 MHz	1
CC1000DK-868	CC1000 Development Kit, 868/915 MHz	1
CC1000SK	CC1000 Sample Kit (5 pcs)	1

MOQ = Minimum Order Quantity

Address:
Chipcon AS
Gaustadalléen 21
N-0349 Oslo,
NORWAY

Telephone : (+47) 22 95 85 44
Fax : (+47) 22 95 85 46
E-mail : wireless@chipcon.com
Web site : http://www.chipcon.com

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